EE 330 Fall 2023 Rm 1012 Coover

	1	2	3	4	5	6	7	8	ROW
1	Ethan Hulinski	Calvin Mitchell	Adam Shoberg	Henry Chamberlain	Peter Hurd	Nathan Cook	Joseph Dicklin		1
2	Julia Falat	Kendyl Chermak	Alec Sutton	Austyn Shrader	Astha Upadhyay	Lalitha Vattyam	Eileen Hillier	Nicholas Lynch	2
3	Tarun Srikaran	Julia Kroeper	Yu Wei Tan	Haris Khan	Zachary Hainline	Carter Murawski	Marek Jablonski	Jonah Frosch	3
4			Cullen White	Evan Rosonke		Sean Gray		John Lavigne	4
5									5
6									6

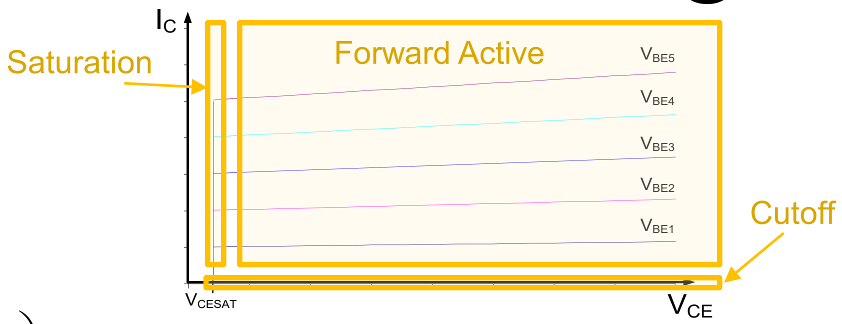
EE 330
Lecture 21

- Bipolar Process

Fall 2023 Exam Schedule

Exam 1	Friday Sept 22	
Exam 2	Friday Oct 20	
Exam 3	Friday Nov. 17	
Final	Monday Dec 11	12:00 – 2:00 p.m.

Simplified Multi-Region Model



$$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}}\left(1+\frac{V_{CE}}{V_{AF}}\right)$$

$$I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}} \qquad V_t = \frac{kT}{q}$$

Forward Active

V_{BE}=0.7V
V_{CE}=0.2V

Saturation

I_C=I_B=0

Cutoff

- This is a piecewise model suitable for analytical calculations
- Can easily extend to reverse active mode but of little use
- Still need conditions for operating in the 3 regions

Review from Last Lecture

Simplified Multi-Region Model

Alternate equivalent model

Model	Conditions	Region
$I_C = \beta I_B\left(1+\frac{V_{CE}}{V_{AF}}\right)$ $I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$ $V_t = \frac{kT}{q}$	$V_{BE}>0.4V$ $V_{BC}<0$	Forward Active
$V_{BE}=0.7V$ $V_{CE}=0.2V$	$I_C<\beta I_B$	Saturation
$I_C=I_B=0$	$V_{BE}<0$ $V_{BC}<0$	Cutoff

A small portion of the operating region is missed with this model but seldom operate in the missing region

Further Simplified Multi-Region dc Model

Equivalent Further Simplified Multi-Region Model

$I_C = \beta I_B$ $V_{BE} = 0.6V$ $V_t = \frac{kT}{q}$	$V_{BE}>0.4V$ $V_{BC}<0$	Forward Active
$V_{BE}=0.7V$ $V_{CE}=0.2V$	$I_C<\beta I_B$	Saturation
$I_C=I_B=0$	$V_{BE}<0$ $V_{BC}<0$	Cutoff

A small portion of the operating region is missed with this model but seldom operate in the missing region

Bipolar Process Description

p-substrate epi

Components Shown

- Vertical npn BJT
- Lateral pnp BJT
- JFET
- Diffusion Resistor
- Diode (and varactor)

Note: Features intentionally not to scale to make it easier to convey more information on small figures

- Much processing equipment is same as used for MOS processes so similar minimum-sized features can be made

- But will see that there are some fundamental issues that typically make bipolar circuits large

TABLE 2C.1
Process scenario of major process steps in typical bipolar process[a]

1.	Clean wafer (p-type)	
2.	GROW THIN OXIDE	
3.	Apply photoresist	
4.	PATTERN n^+ BURIED LAYER	(MASK #1)
5.	Develop photoresist	
6.	DEPOSITION AND DIFFUSION OF n-BURIED LAYER	
7.	Strip photoresist	
8.	Strip oxide	
9.	GROW EPITAXIAL LAYER (n-type)	
10.	Grow oxide	
11.	Apply photoresist	
12.	PATTERN p^+ ISOLATION REGIONS	(MASK #2)
13.	Develop photoresist	
14.	Etch oxide	
15.	DEPOSITION AND DIFFUSION OF p^+ ISOLATION	
16.	Strip photoresist	
17.	Grow oxide	
	Optional high-resistance p-diffusion	
	A.1 Apply photoresist	
	A.2 PATTERN p-RESISTORS	(MASK #A)
	A.3 Develop photoresist	
	A.4 Etch oxide	
	A.5 DEPOSITION AND DIFFUSION OF p-RESISTORS	
	A.6 Strip photoresist	
	A.7 Grow oxide	
18.	Apply photoresist	
19.	PATTERN BASE REGIONS	(MASK #3)
20.	Develop photoresist	
21.	Etch oxide	
22.	DEPOSITION AND DIFFUSION OF p-TYPE BASE	
23.	Strip photoresist	
24.	Grow oxide	
25.	Apply photoresist	

26. PATTERN n-TYPE EMITTER REGIONS (MASK #4)
27. Develop photoresist
28. Etch Oxide
29. n^+ DEPOSITION AND DIFFUSION
30. Strip photoresist
31. Grow oxide
32. Apply photoresist
33. PATTERN CONTACT OPENINGS (MASK #5)
34. Develop photoresist
35. Etch oxide
36. Strip Photoresist
37. APPLY METAL
38. Apply photoresist
39. PATTERN METAL (MASK #6)
40. Develop photoresist
41. ETCH METAL
42. Strip photoresist
43. APPLY PASSIVATION
44. Apply photoresist
45. PATTERN PAD OPENINGS (MASK #7)
46. Develop photoresist
47. Etch passivation
48. Strip photoresist
49. ASSEMBLE, PACKAGE, AND TEST

- Small number of masks
- Most not critical alignment / size

TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5\ \mu$)
(See Table 2C.3 in color plates for graphical interpretation)

	Dimension
1. n^+ buried collector diffusion (Yellow, Mask #1)	
1.1 Width	3λ
1.2 Overlap of p-base diffusion (for vertical npn)	2λ
1.3 Overlap of n^+ emitter diffusion (for collector contact of vertical npn)	2λ
1.4 Overlap of p-base diffusion (for collector and emitter of lateral pnp)	2λ
1.5 Overlap of n^+ emitter diffusion (for base contact of lateral pnp)	2λ
2. Isolation diffusion (Orange, Mask #2)	
2.1 Width	4λ
2.2 Spacing	24λ
2.3 Distance to n^+ buried collector	14λ
3. p-base diffusion (Brown, Mask #3)	
3.1 Width	3λ
3.2 Spacing	5λ
3.3 Distance to isolation diffusion	14λ
3.4 Width (resistor)	3λ
3.5 Spacing (as resistor)	3λ
4. n^+ emitter diffusion (Green, Mask #4)	
4.1 Width	3λ
4.2 Spacing	3λ
4.3 p-base diffusion overlap of n^+ emitter diffusion (emitter in base)	2λ
4.4 Spacing to isolation diffusion (for collector contact)	12λ
4.5 Spacing to p-base diffusion (for base contact of lateral pnp)	6λ
4.6 Spacing to p-base diffusion (for collector contact of vertical npn)	6λ

- Note some features have very large design rules
- Will discuss implication of this later

5. Contact (Black, Mask #5)	
5.1 Size (exactly)	$4\lambda \times 4\lambda$
5.2 Spacing	2λ
5.3 Metal overlap of contact	λ
5.4 n^+ emitter diffusion overlap of contact	2λ
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
5.7 Spacing to isolation diffusion	4λ
6. Metalization (Blue, Mask #6)	
6.1 Width	2λ
6.2 Spacing	2λ
6.3 Bonding pad size	$100\ \mu \times 100\ \mu$
6.4 Probe pad size	$75\ \mu \times 75\ \mu$
6.5 Bonding pad separation	$50\ \mu$
6.6 Bonding to probe pad	$30\ \mu$
6.7 Probe pad separation	$30\ \mu$
6.8 Pad to circuitry	$40\ \mu$
6.9 Maximum current density	0.8 mA/μ width
7. Passivation (Purple, Mask #7)	
7.1 Minimum bonding pad opening	$90\ \mu \times 90\ \mu$
7.2 Minimum probe pad opening	$65\ \mu \times 65\ \mu$

5. Contact (Black, Mask #5)

5.1 Size (exactly)	$4\lambda \times 4\lambda$
5.2 Spacing	2λ
5.3 Metal overlap of contact	λ
5.4 n^+ emitter diffusion overlap of contact	2λ
5.5 p-base diffusion overlap of contact	2λ
5.6 p-base to n^+ emitter	3λ
	4λ

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2
6.2	Minimum active overlap	1.5	1.5	1.5
6.3	Minimum contact spacing	2	3	4
6.4	Minimum spacing to gate of transistor	2	2	2

2λ

2λ

$100\ \mu \times 100\ \mu$

$75\ \mu \times 75\ \mu$

$50\ \mu$

$30\ \mu$

$30\ \mu$

$40\ \mu$

0.8 mA/μ width

$90\ \mu \times 90\ \mu$

$65\ \mu \times 65\ \mu$

TABLE 2C.4

Process parameters for a typical bipolar process[a]

Parameter	Typical	Tolerance[b]	Units
	Ebers-Moll model parameters		
β_F (forward β)			
npn—vertical	100	50 to 200	
pnp—lateral			
(at $I_C = 500\ \mu A$)	10	±20%	
(at $I_C = 200\ \mu A$)	6	±20%	
β_R (reverse β)			
npn—vertical	1.5	±0.5	
pnp—lateral			
(at $I_C = 500\ \mu A$)	5	±20%	
(at $I_C = 200\ \mu A$)	3	±20%	
V_{AF} (forward Early voltage)			
npn—vertical	100	±30%	V
pnp—lateral	150	±30%	V
V_{AR} (reverse Early voltage)			
npn—vertical	150	±30%	V
pnp—lateral	150	±30%	V
J_S (saturation current density)			
npn—vertical	2.6×10^{-7}	−50%to + 100%	pA/μ^2
pnp—lateral	1.3×10^{-5}	−50%to + 100%	pA/μ emitter perimeter

Parameter	Typical	Tolerance[b]	Units
Doping			
n^+ emitter	10^4	±30%	$10^{16}/cm^3$
p-base			
Surface	10^5	±20%	$10^{16}/cm^3$
Junction	1	±20%	$10^{16}/cm^3$
Epitaxial layer	0.3	±20%	$10^{16}/cm^3$
Substrate	0.08	±25%	$10^{16}/cm^3$
Physical feature size			
Diffusion depth			
n+ emitter diffusion	1.3	±5%	μ
p-base diffusion	2.6	±5%	μ
p-resistive diffusion	0.3	±5%	μ
n-epitaxial layer	10.4	±5%	μ
n^+ buried collector diffusion			
Into epitaxial	3.9	±5%	μ
Into substrate	7.8	±5%	μ
Oxide thickness			
Metal to epitaxial	1.4	±30%	μ
Metal to p-base	0.65	±30%	μ
Metal to n^+ emitter	0.4	±30%	μ

Capacitances

Metal to epitaxial	0.022	±30%	fF/μ^2
Metal to p-base diffusion	0.045	±30%	fF/μ^2
Metal to n^+ emitter diffusion	0.078	±30%	fF/μ^2
n^+ buried collector to substrate (junction, bottom)	0.062	±30%	fF/μ^2
Epitaxial to substrate (junction, bottom)	0.062	±30%	fF/μ^2
Epitaxial to substrate (junction, sidewall)	1.6	±30%	fF/μ perimeter
Epitaxial to p-base diffusion (junction, bottom)	0.14	±30%	fF/μ^2
Epitaxial to p-base diffusion (junction, sidewall)	7.9	±30%	fF/μ perimeter
p-base diffusion to n^+ emitter diffusion (junction, bottom)	0.78	±30%	fF/μ^2
p-base diffusion to n^+ emitter diffusion (junction, sidewall)	3.1	±30%	fF/μ perimeter

Parameter	Typical	Tolerance[b]	Units
Resistance and resistivity			
Substrate resistivity	16	±25%	Ω · cm
n^+ buried collector diffusion	17	±35%	Ω / □
Epitaxial layer	1.6	±20%	Ω · cm
p-base diffusion	160	±20%	Ω / □
p-resistive diffusion (optional)	1500	±40%	Ω / □
n^+ emitter diffusion	4.5	±30%	Ω / □
Metal	0.003		Ω / □
Contacts ($3\mu \times 3\mu$)	<4		Ω
Metal-n^+ emitter (contact plus series resistance to BE junction)	<1		Ω
Metal-p-base[c] (contact plus series resistance)	70		Ω
Metal-Epitaxial[d] (contact plus series resistance to BC junction)	120		Ω
Breakdown voltages, leakage currents, migration currents, and operating conditions			
Reverse breakdown voltages			
n^+ emitter to p-base	6.9	±50 mV	V
p-base to epitaxial	70	±10	V
Epitaxial to substrate	>80		V
Maximum operating voltage	40		V
Substrate leakage current	0.16		fA/μ^2
Maximum metal current density	0.8		mA/μ width
Maximum device operating temperature (design)	125		°C
Maximum device operating temperature (physical)	225		°C

SPICE model parameters of typical bipolar process

Parameter[a,b,c]	Vertical npn	Lateral pnp	Units
IS[c]	0.1	0.78	fA
BF	80	225	
NF	1	1	
VAF	100	150	V
IKF	100	0.1	mA
ISE	0.11	0.15	fA
NE	1.44	1.28	
BR	1.5		
NR	1	1	
VAR[b]	19	38	V
ISC		1.5	fA
NC	1.44	1.28	
RB	70	250	Ω
RE	1	4	Ω
RC	120	130	Ω
CJE	0.62	0.48	pF
VTE	0.69	0.65	V
MJE	0.33	0.40	
TF	0.45	40	ns
CJC	1.9	0.48	pF
VJC	0.65	0.65	V
MJC	0.4	0.4	
XCJC	0.5	0	
TR	22.5	2000	ns
CJS[d]	1.30	0	pF
VJS	0.49	0	pF
MJS	0.38	0	

Recall: Simplified Multi-Region Model

"Forward" Regions : $\beta=\beta_F$

	Conditions	
$I_C = J_S A_E e^{\frac{V_{BE}}{V_t}}\left(1+\frac{V_{CE}}{V_{AF}}\right)$ $I_B = \frac{J_S A_E}{\beta} e^{\frac{V_{BE}}{V_t}}$	$V_{BE}>0.4V$ $V_{BC}<0$	Forward Active
$V_{BE}=0.7V$ $V_{CE}=0.2V$	$I_C<\beta I_B$	Saturation
$I_C=I_B=0$	$V_{BE}<0$ $V_{BC}<0$	Cutoff

Process Parameters: $\{J_S, \beta, V_{AF}\}$ $V_t = \frac{kT}{q}$ Design Parameters: $\{A_E\}$

- Process parameters highly process dependent
- J_S highly temperature dependent as well, β modestly temperature dependent
- This model is dependent only upon emitter area, independent of base and collector area !
- Currents scale linearly with A_E and not dependent upon shape of emitter
- A small portion of the operating region is missed with this model but seldom operate in the missing region

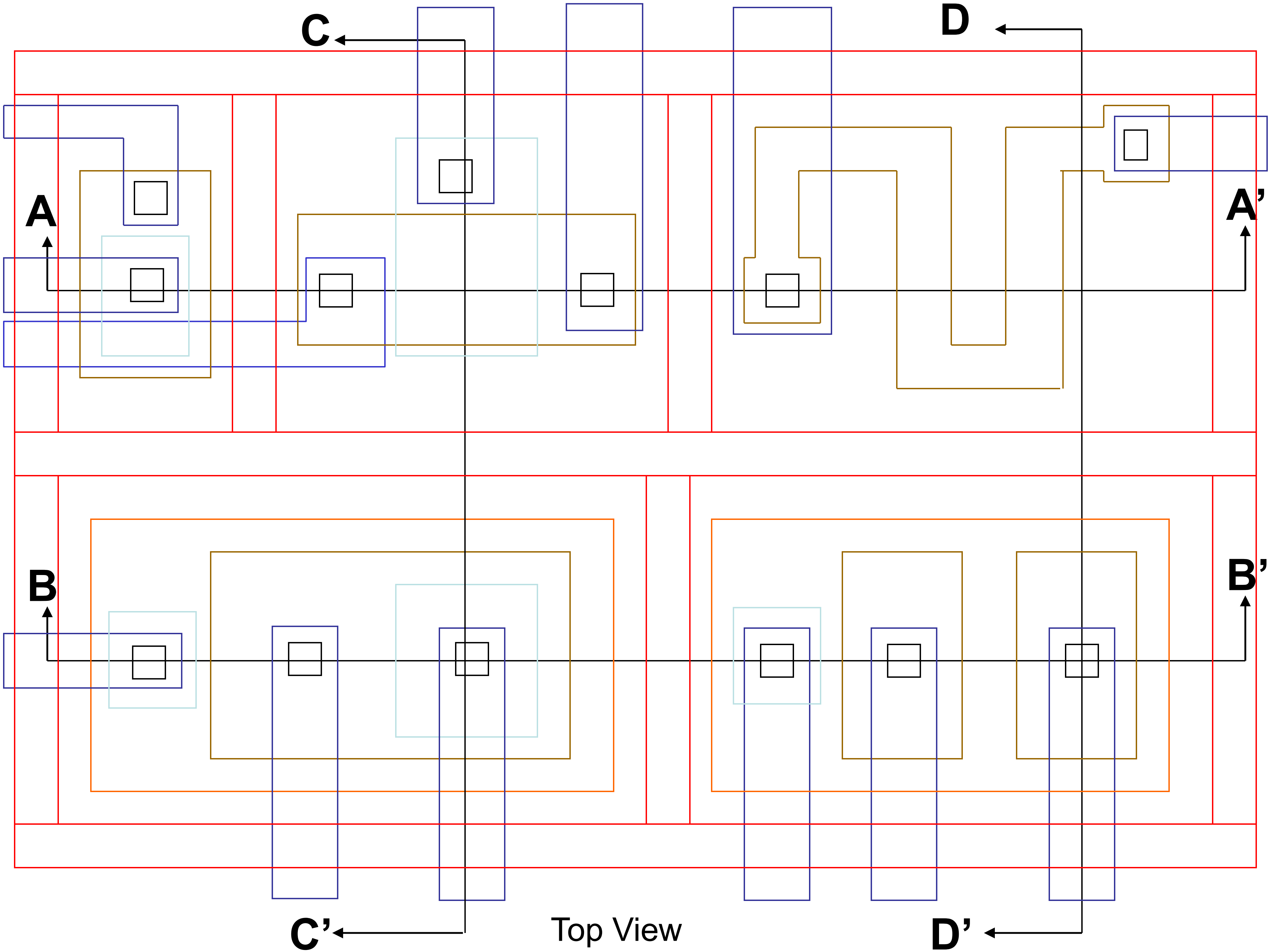
[a]Parameters are defined in Chapters 3 and 4.

[b]Some of these Gummel-Poon parameters differ considerably from those given in Table 2C.4. They have been obtained from curve fitting and should give good results with computer simulations. The parameters of Table 2C.4 should be used for hand analysis.

[c]Parameters that are strongly area-dependent are based upon an npn emitter area of 390 μ^2 and perimeter of 80 μ, a base area of 2200 μ^2 and perimeter of 200 μ, and a collector area of 10,500 μ^2 and perimeter of 425 μ. The lateral pnp has rectangular collectors and emitters spaced 10 μ apart with areas of 230 μ^2 and perimeters of 60 μ. The base area of the pnp is 7400 μ^2 and the base perimeter is 345 μ.

[d]CJS is set to zero for the lateral transistor because it is essentially nonexistent. The parasitic capacitance from base to substrate, which totals 1.0 pF for this device, must be added externally to the BJT.

- In contrast to the MOSFET where process parameters are independent of geometry, the bipolar transistor model is for a specific transistor !
- Area emitter factor is used to model other devices
- Often multiple specific device models are given and these devices are used directly
- Often designer can not arbitrarily set A_E but rather must use parallel combinations of specific devices and layouts

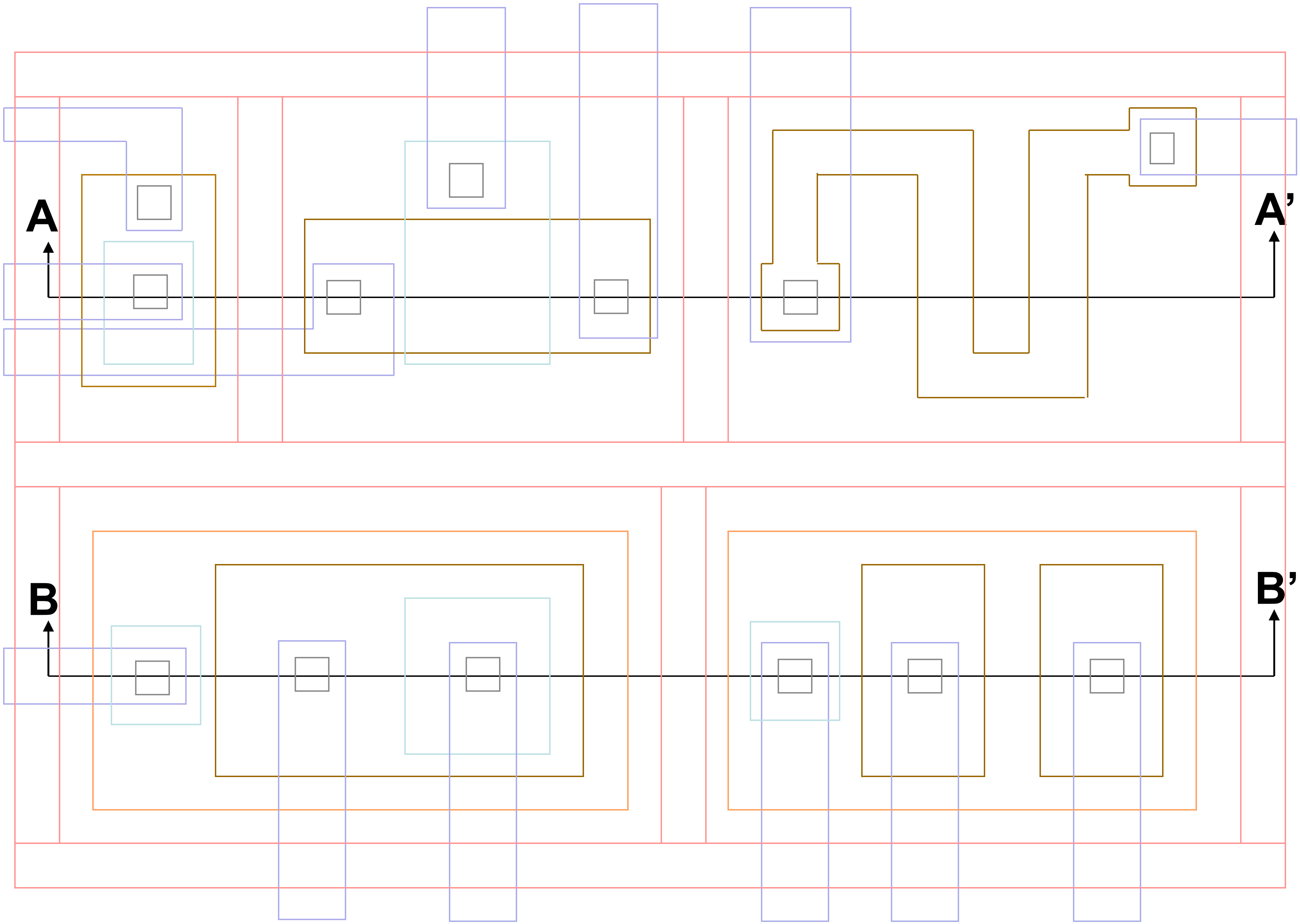


Top View

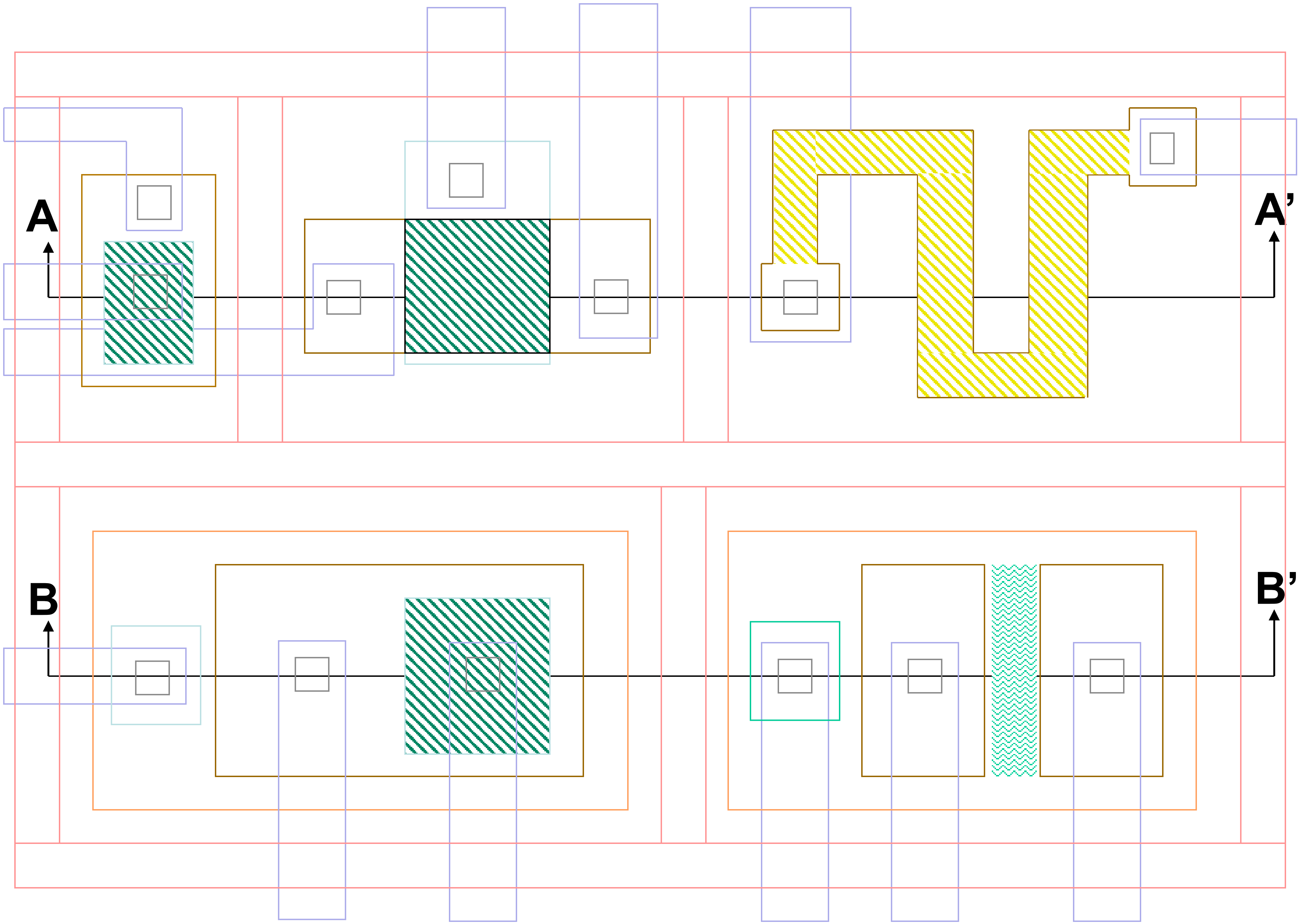
Layer Mappings

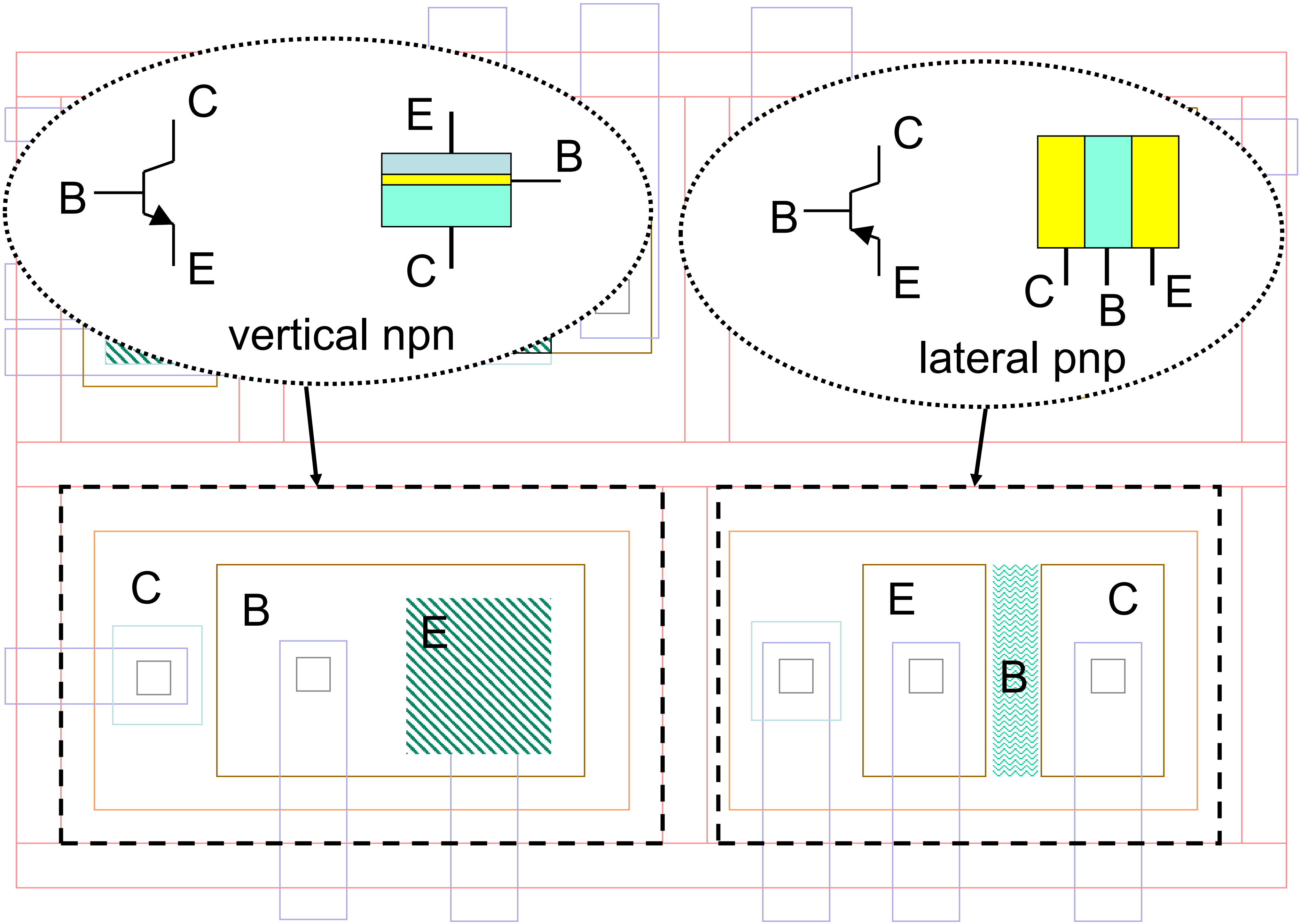
n^+ buried collector
isolation diffusion (p^+)
p-base diffusion
n^+ emitter
contact
metal
passivation opening

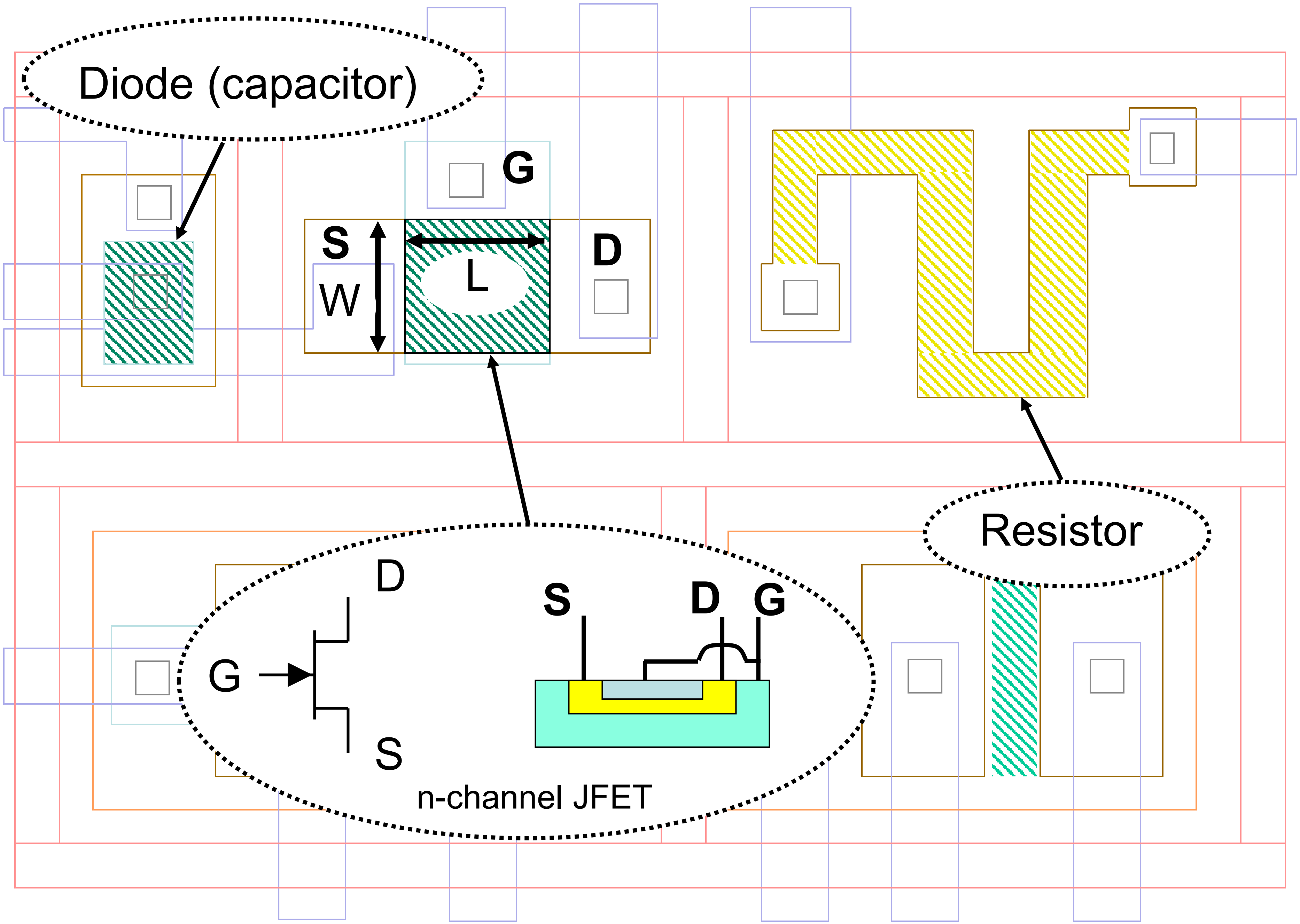
Notes:
- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale



Dimmed features with A-A' and B-B' cross sections


A
A'
B
B'


C
B
E
E
B
C
vertical npn
C
B
E
C
B
E
lateral pnp
C
B
E
E
C
B



Diode (capacitor)
G
S
W
L
D
Resistor
D
G
S
S
D
G
n-channel JFET

Detailed Description of First Photolithographic Steps Only

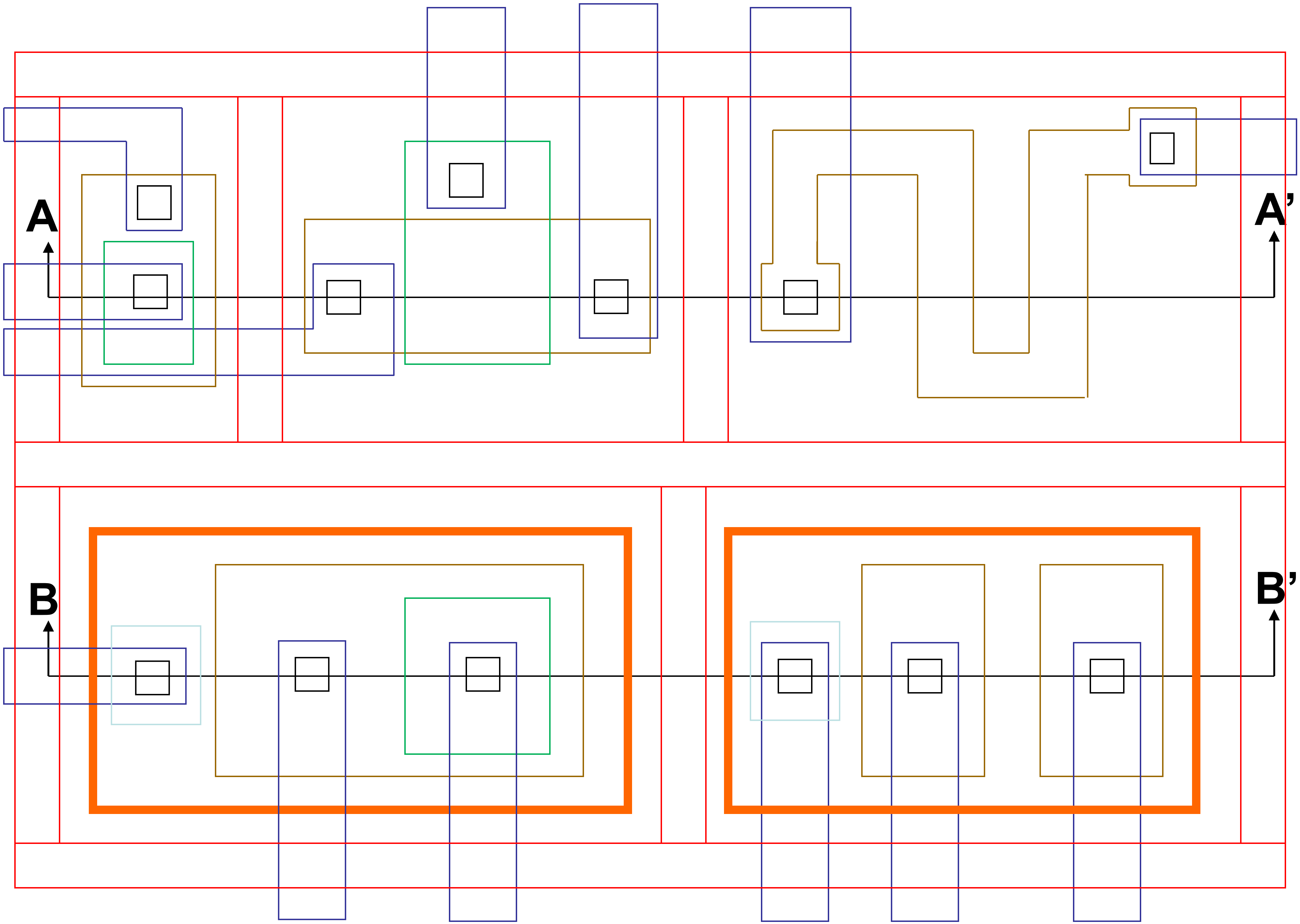
- Top View
- Cross-Section View

Mask Numbering and Mappings

Mask 1	n^+ buried collector
Mask 2	isolation diffusion (p^+)
Mask 3	p-base diffusion
Mask 4	n^+ emitter
Mask 5	contact
Mask 6	metal
Mask 7	passivation opening

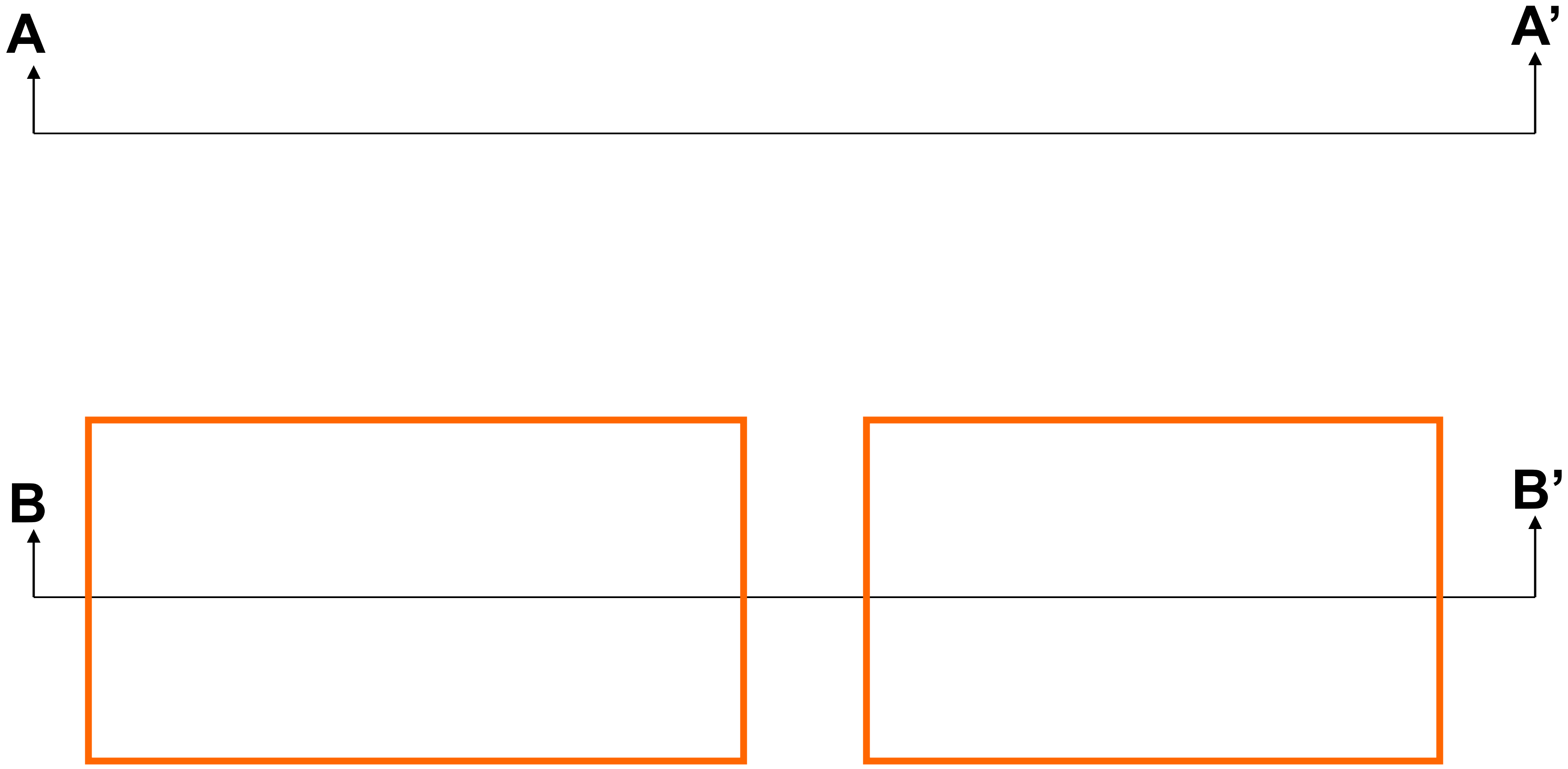
Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale

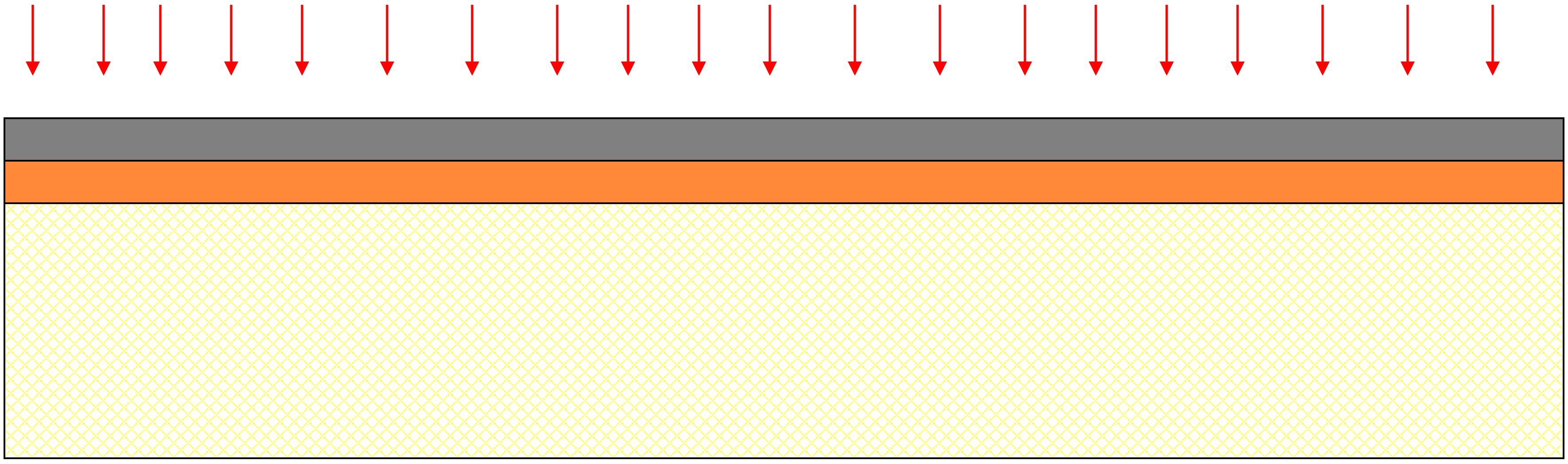


n⁺ buried collector

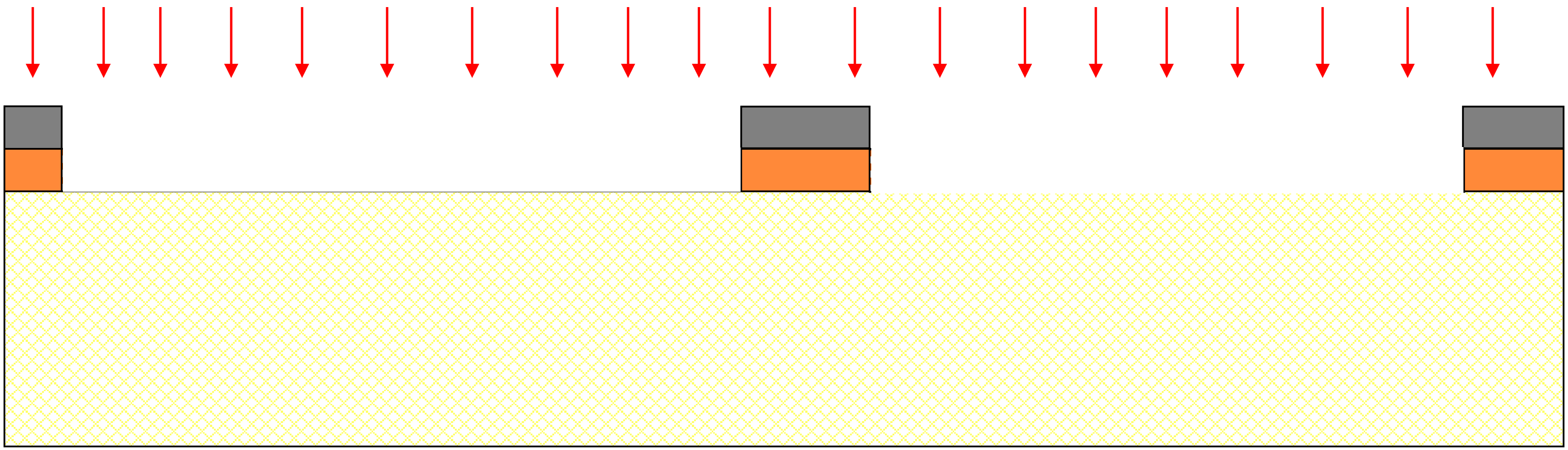
Mask 1: n^+ buried collector



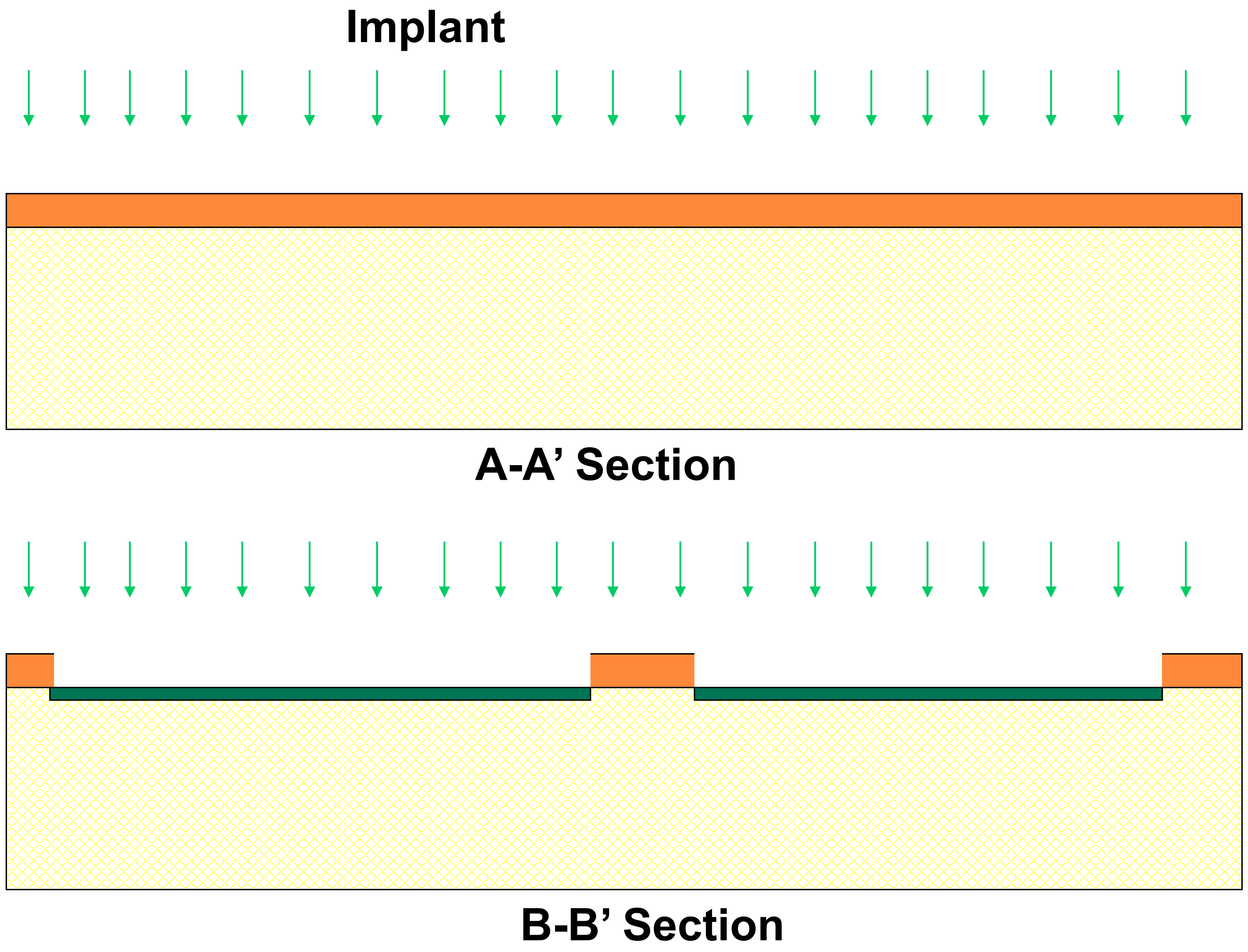
Develop



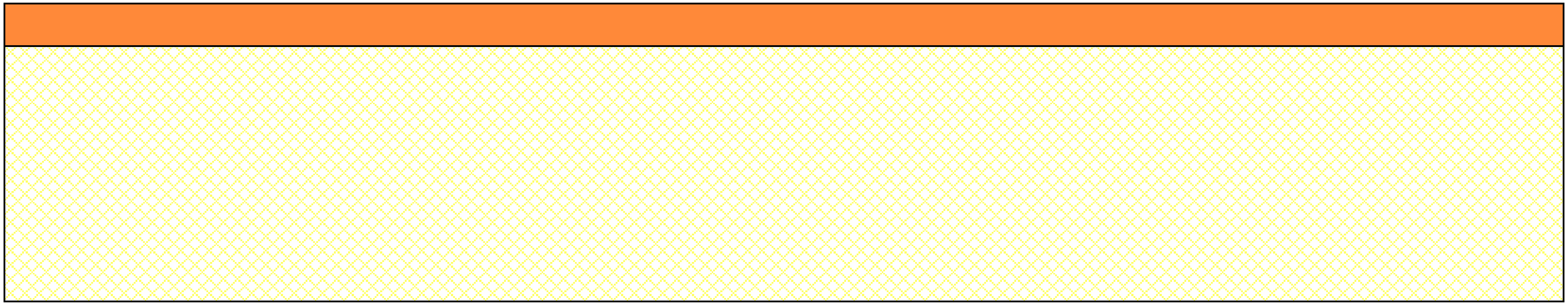
A-A' Section



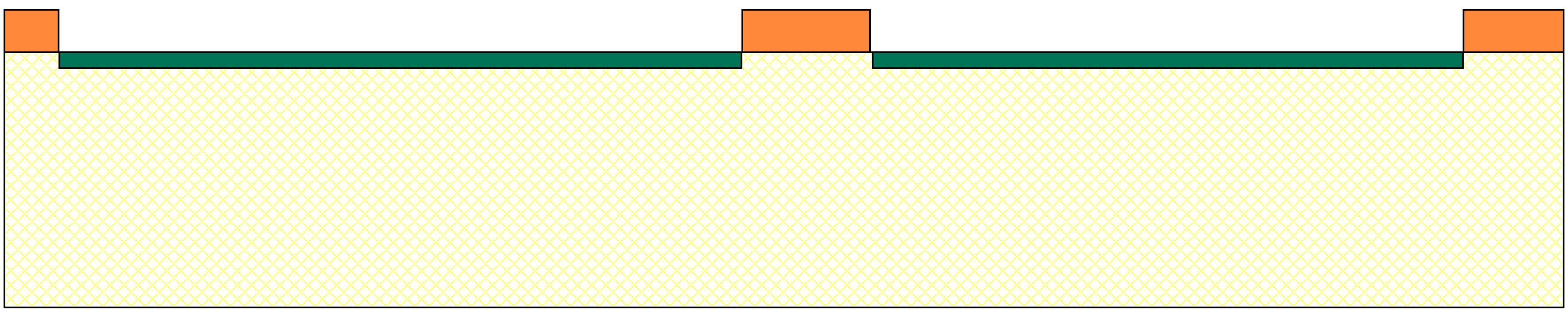
B-B' Section


Implant
A-A' Section
B-B' Section

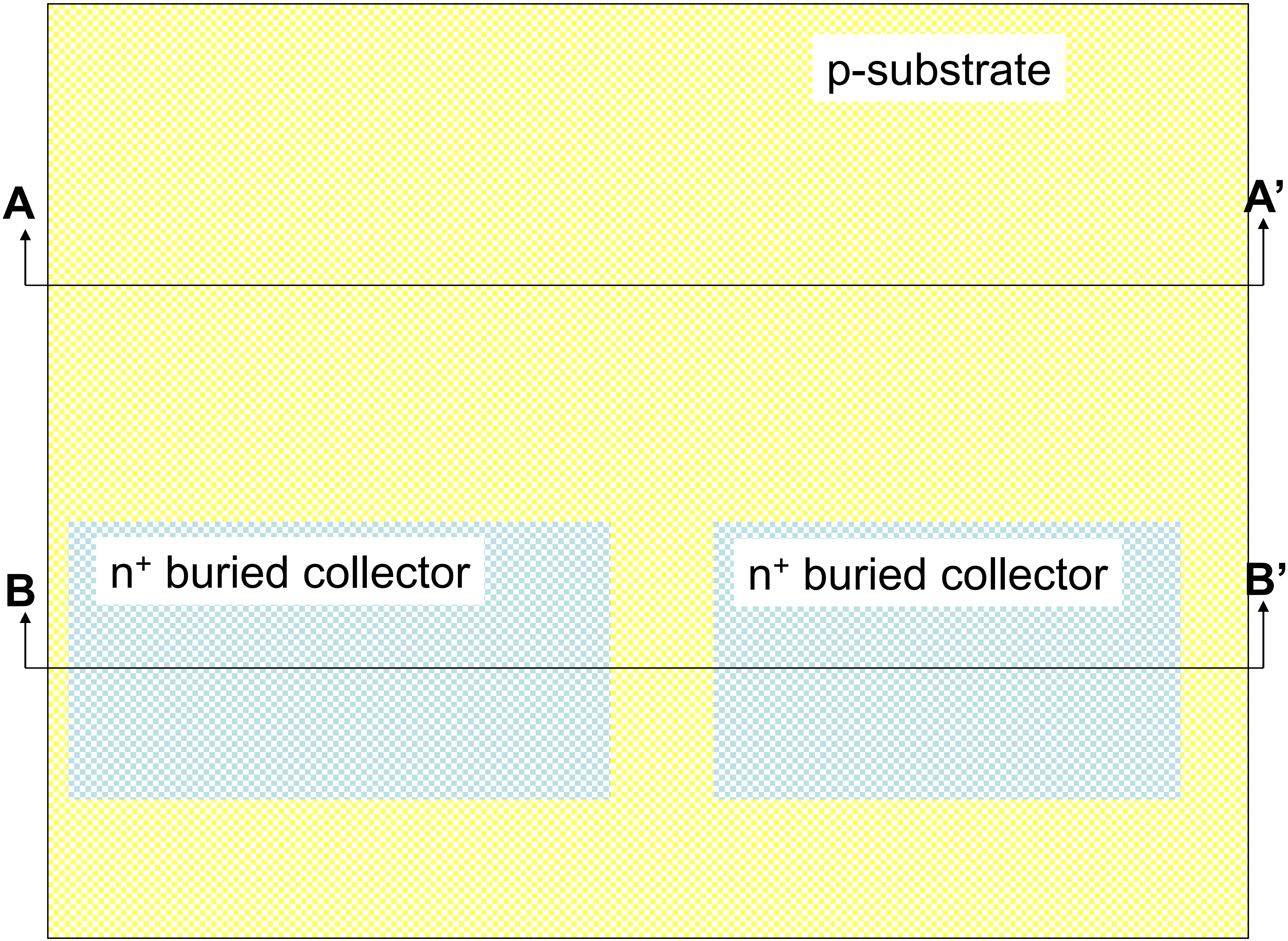
Strip Photoresist



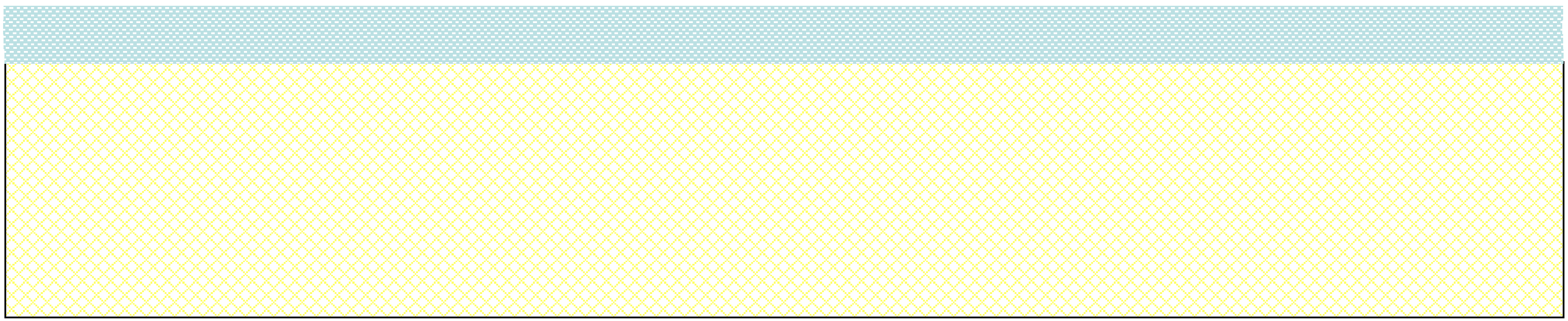
A-A' Section



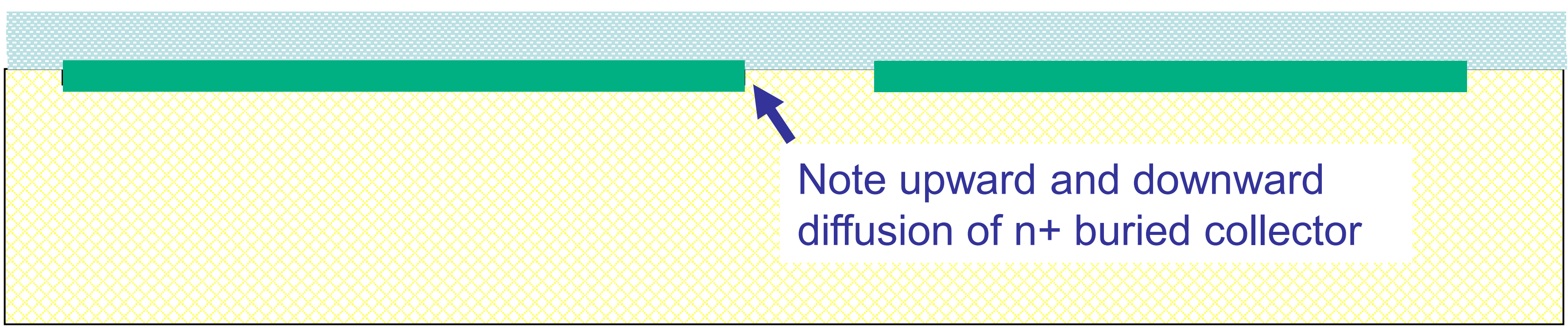
B-B' Section


p-substrate
A
A'
n^+ buried collector
n^+ buried collector
B
B'

Grow Epitaxial Layer

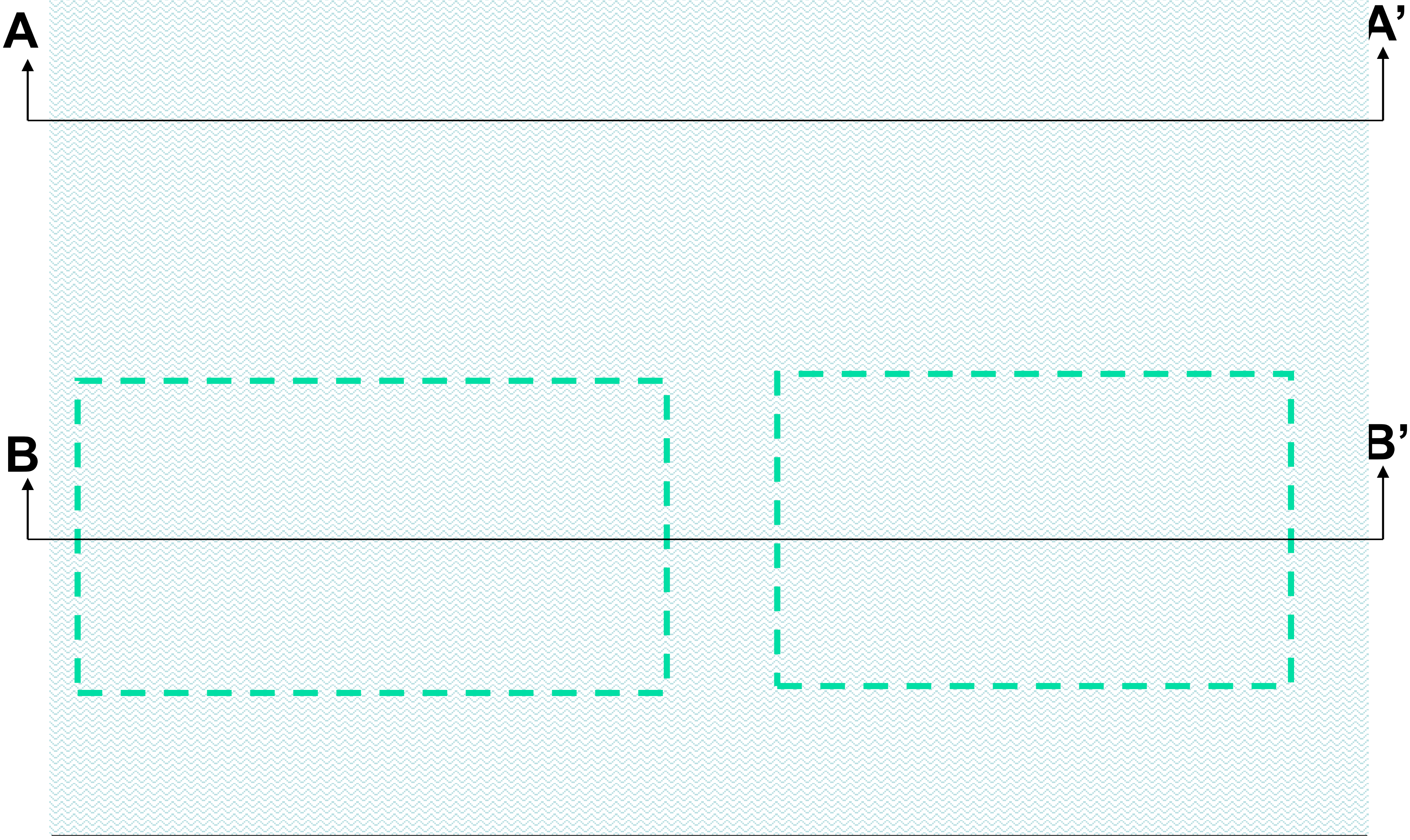


A-A’ Section



B-B’ Section

Grow Epitaxial Layer

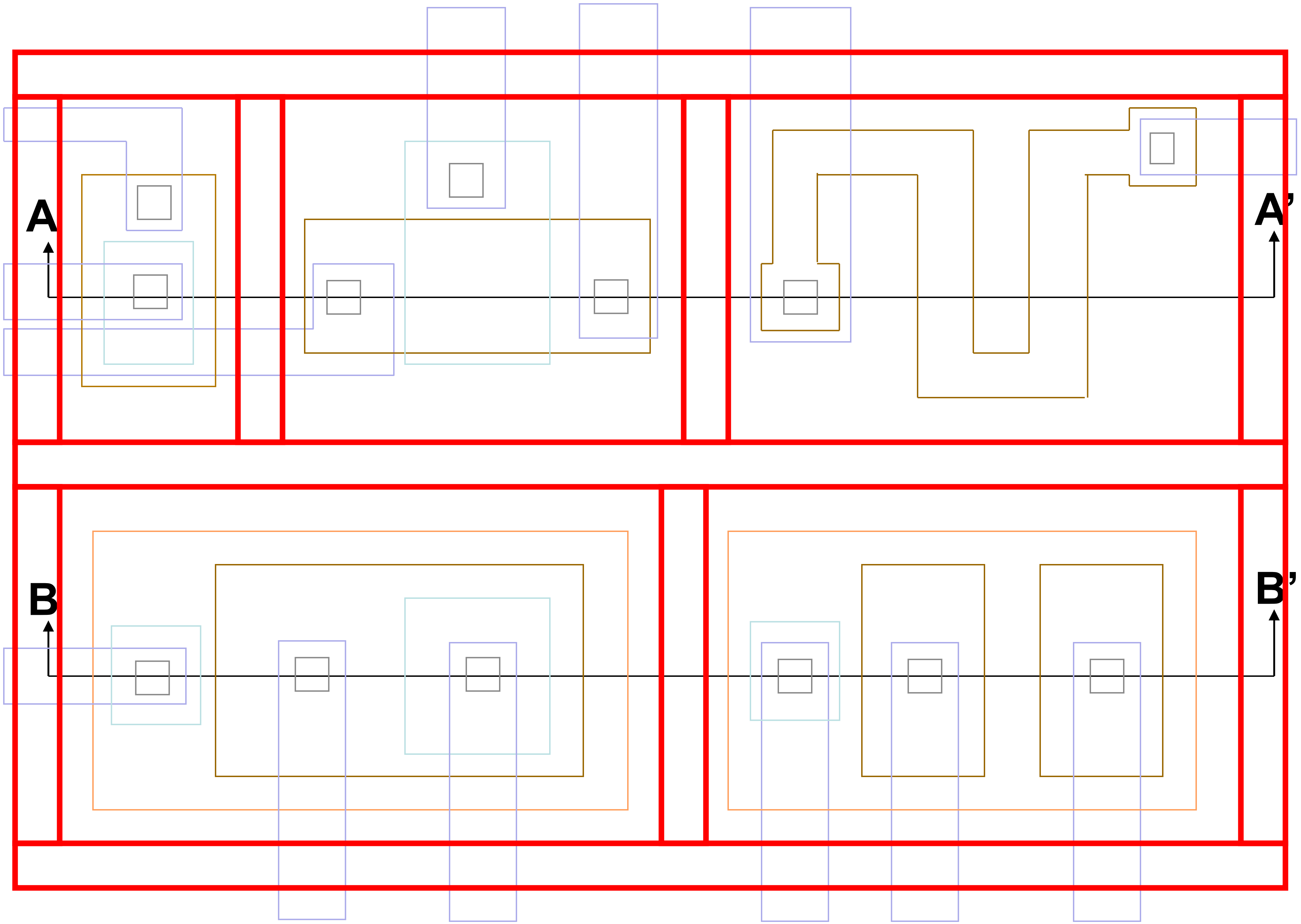


Mask Numbering and Mappings

Mask 1	n^+ buried collector
Mask 2	isolation diffusion (p^+)
Mask 3	p-base diffusion
Mask 4	n^+ emitter
Mask 5	contact
Mask 6	metal
Mask 7	passivation opening

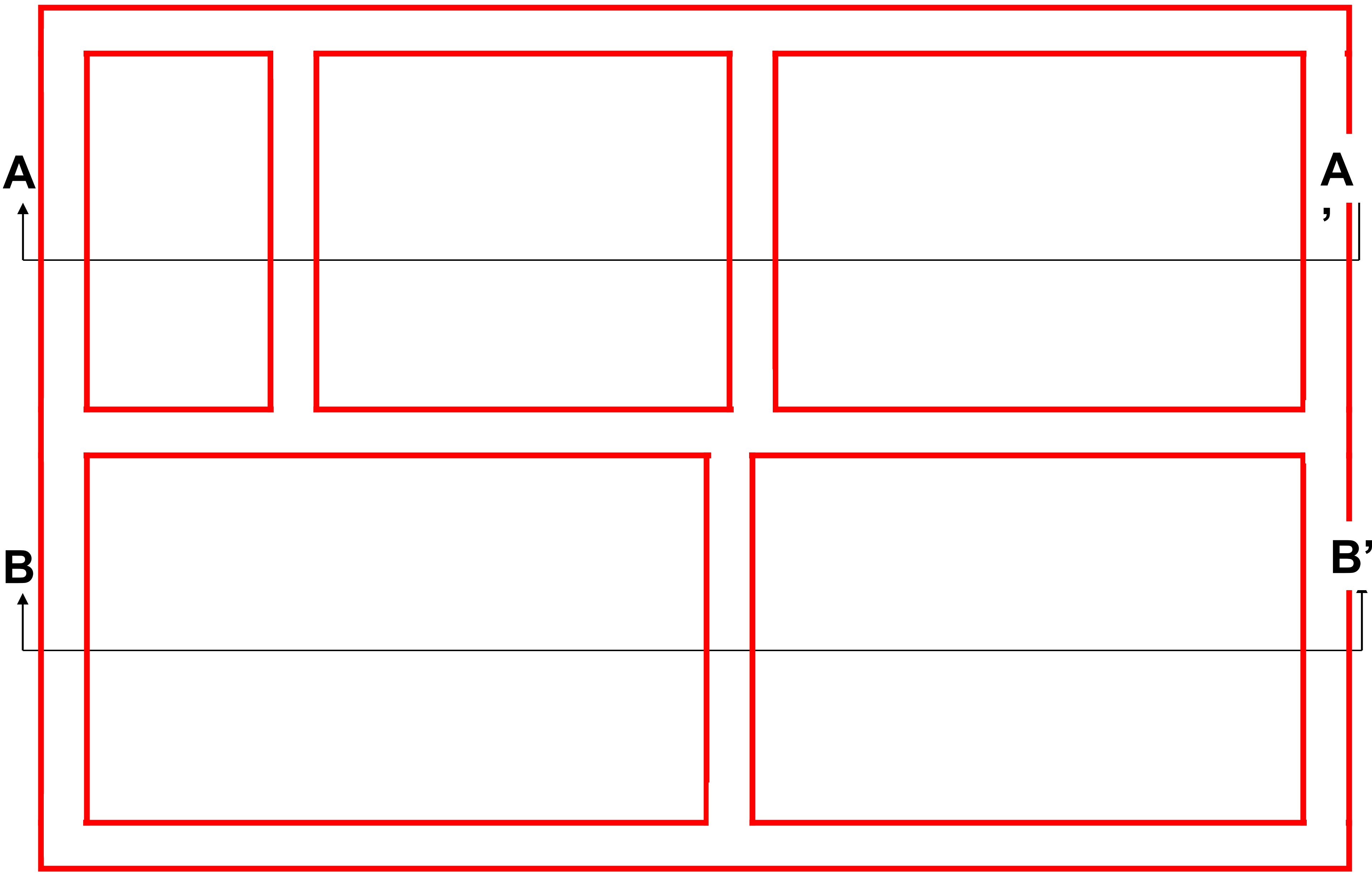
Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale



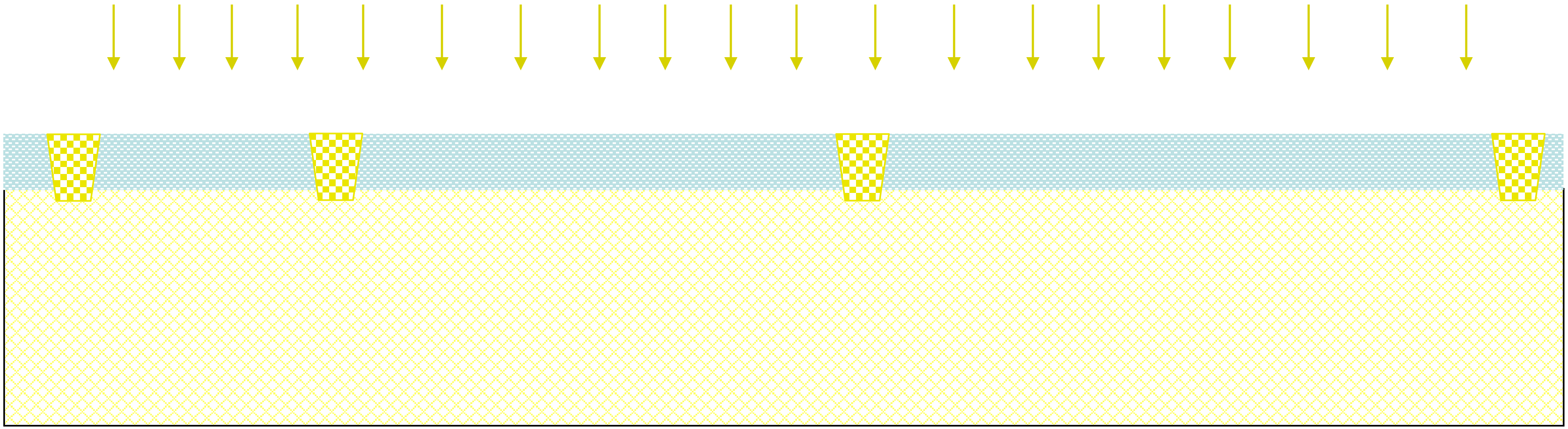
Isolation Diffusion

Mask 2: Isolation Deposition/Diffusion

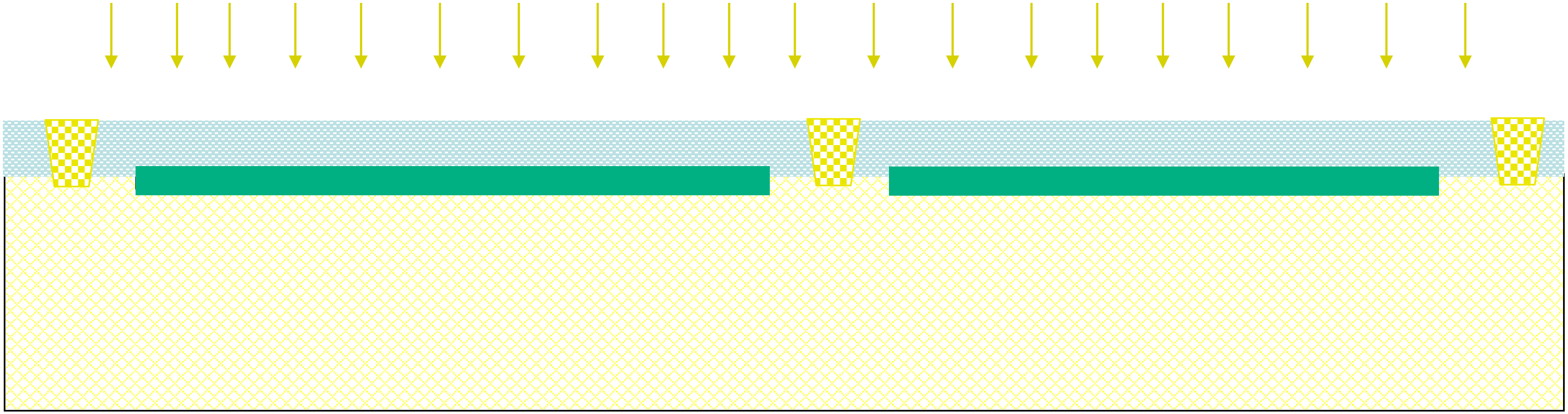


Isolation Deposition/Diffusion

- Photoresist present but not shown
- Deposition and diffusion combined in slides

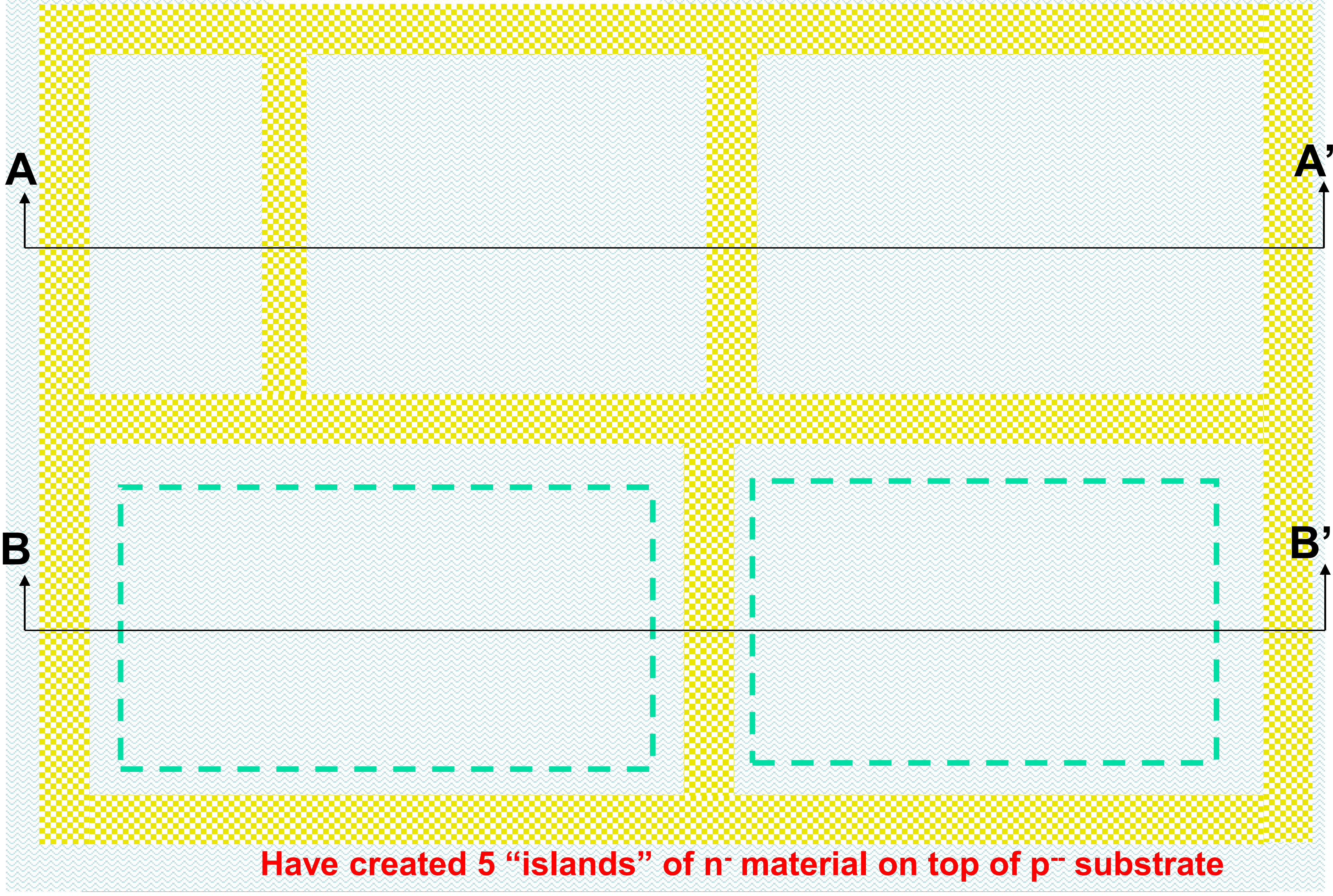


A-A' Section



B-B' Section

Isolation Diffusion



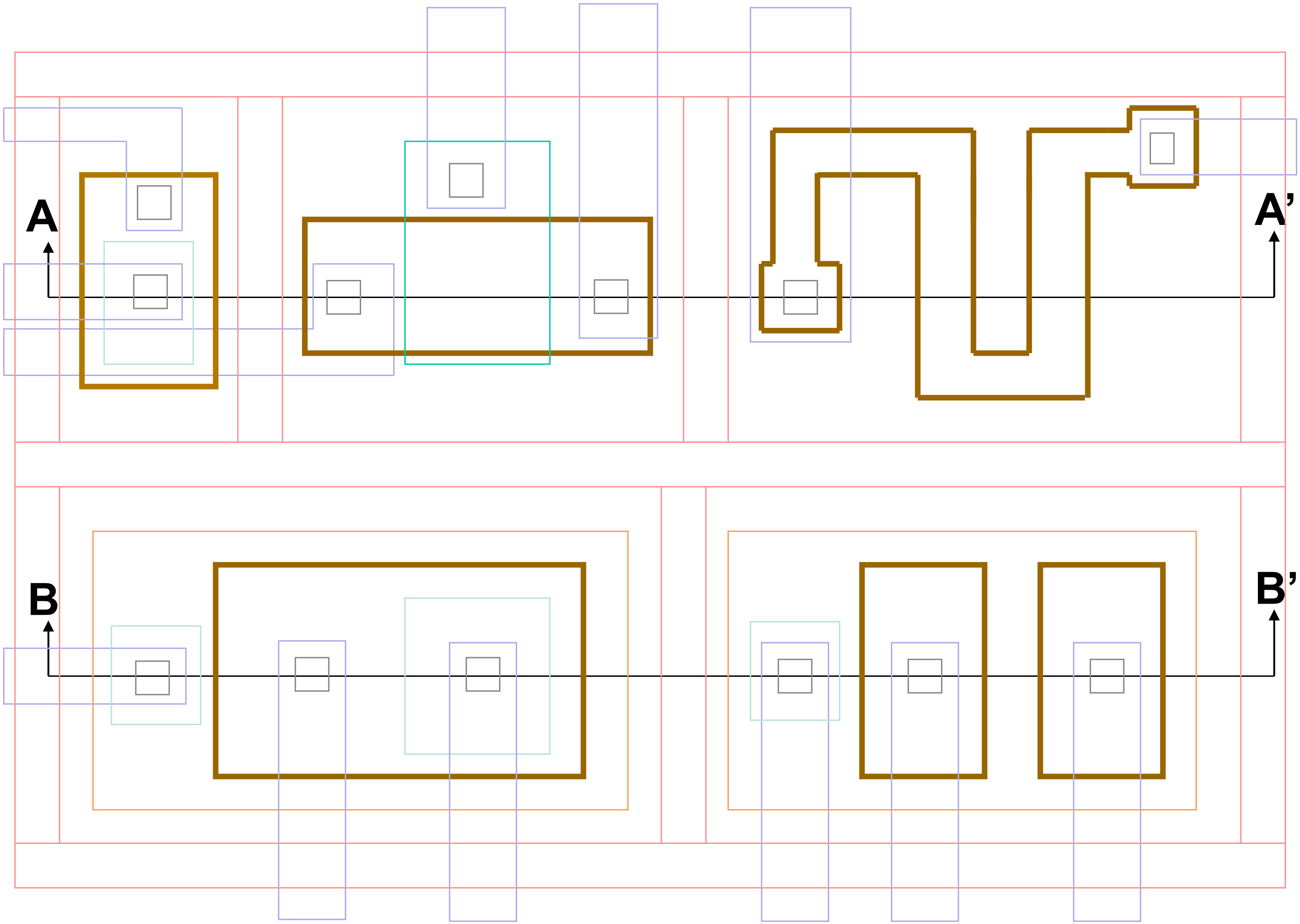
Have created 5 "islands" of n^- material on top of p^{--} substrate

Mask Numbering and Mappings

Mask 1	n^+ buried collector
Mask 2	isolation diffusion (p^+)
Mask 3	p-base diffusion
Mask 4	n^+ emitter
Mask 5	contact
Mask 6	metal
Mask 7	passivation opening

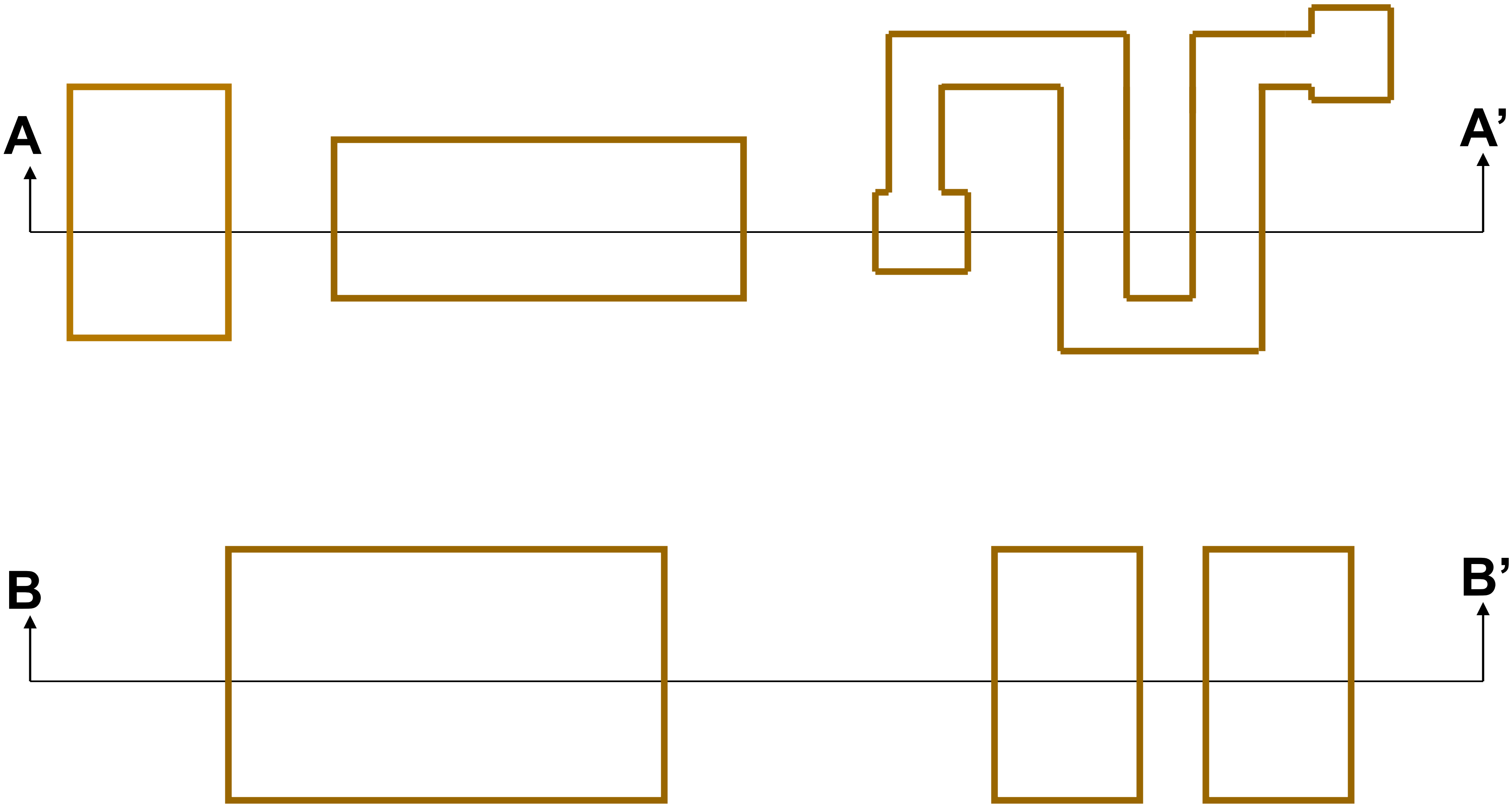
Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale



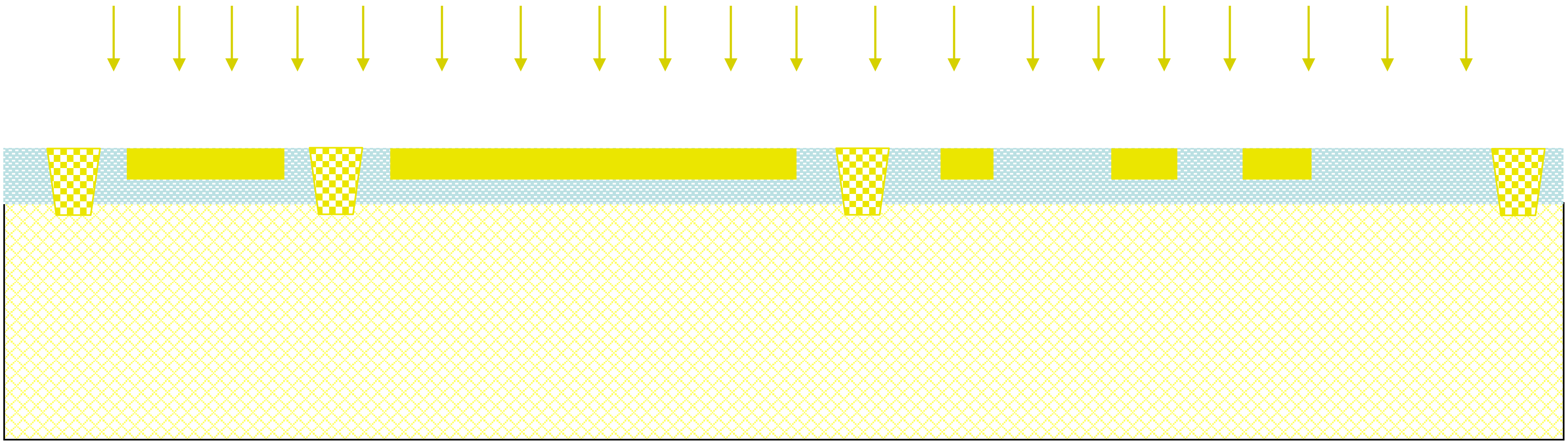
p-base diffusion

Mask 3: p-base diffusion

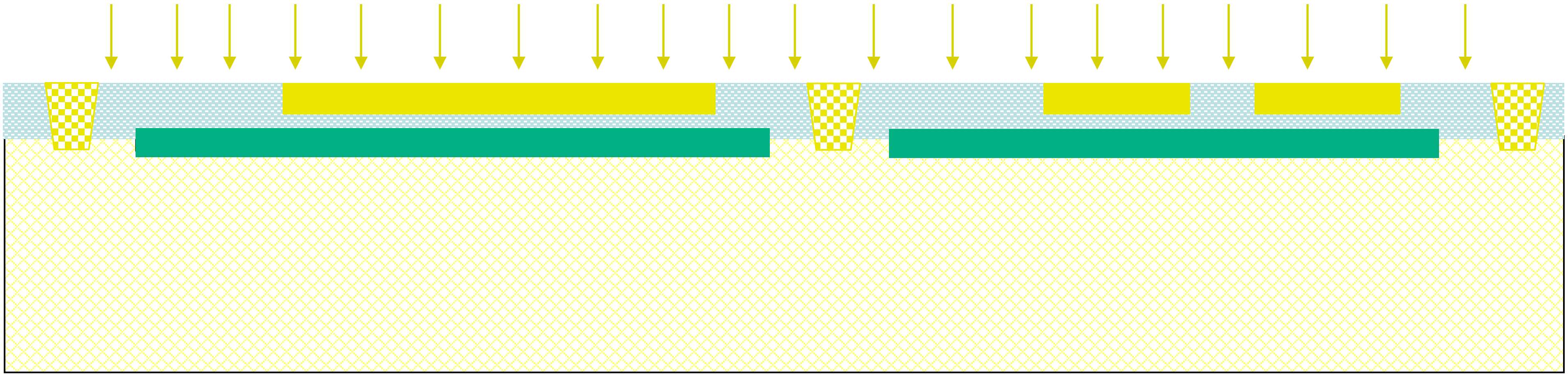


p-base Diffusion

- Photoresist present but not shown
- Deposition and diffusion combined in slides

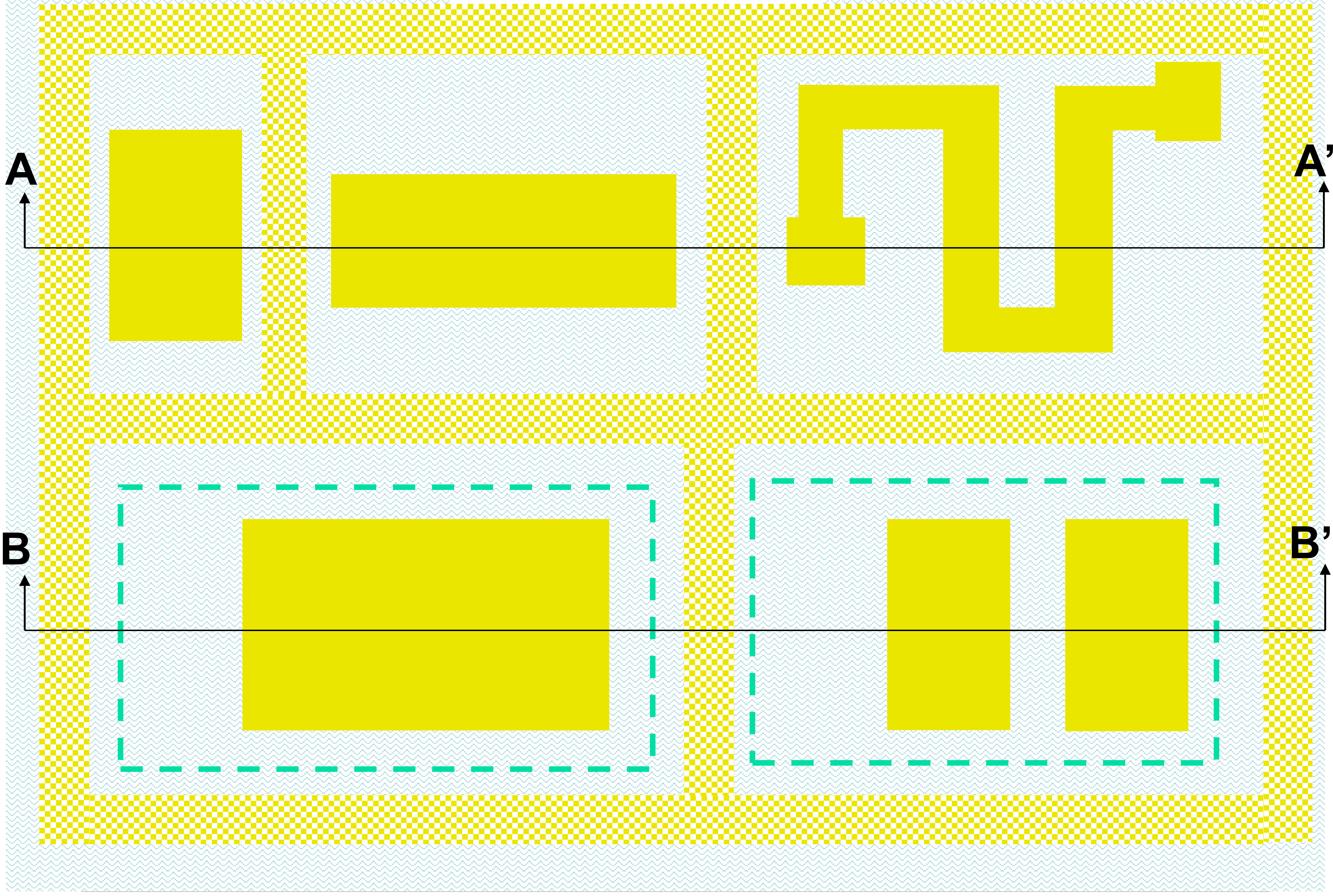


A-A' Section



B-B' Section

p-base Diffusion

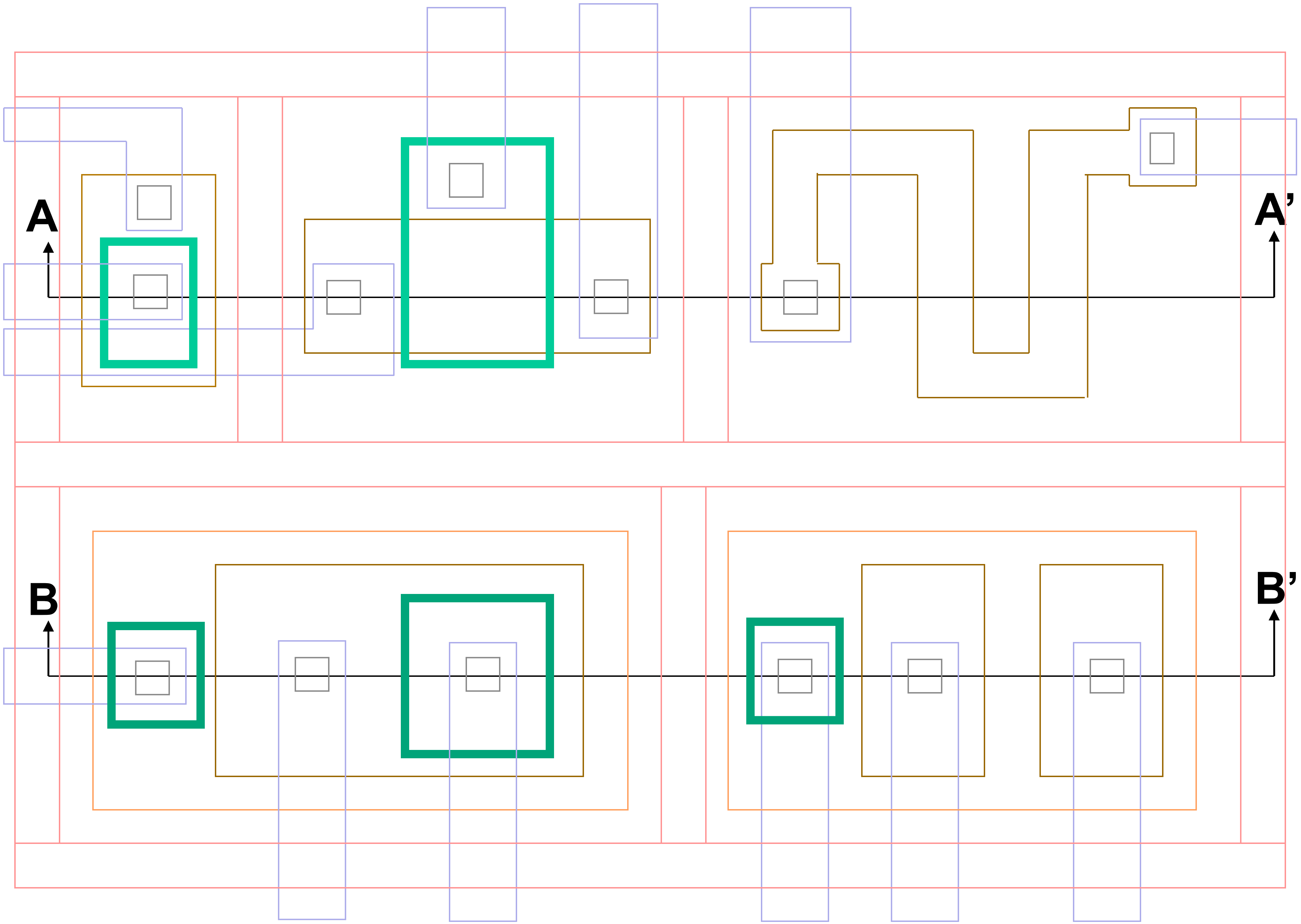


Mask Numbering and Mappings

Mask 1	n^+ buried collector
Mask 2	isolation diffusion (p^+)
Mask 3	p-base diffusion
Mask 4	n^+ emitter
Mask 5	contact
Mask 6	metal
Mask 7	passivation opening

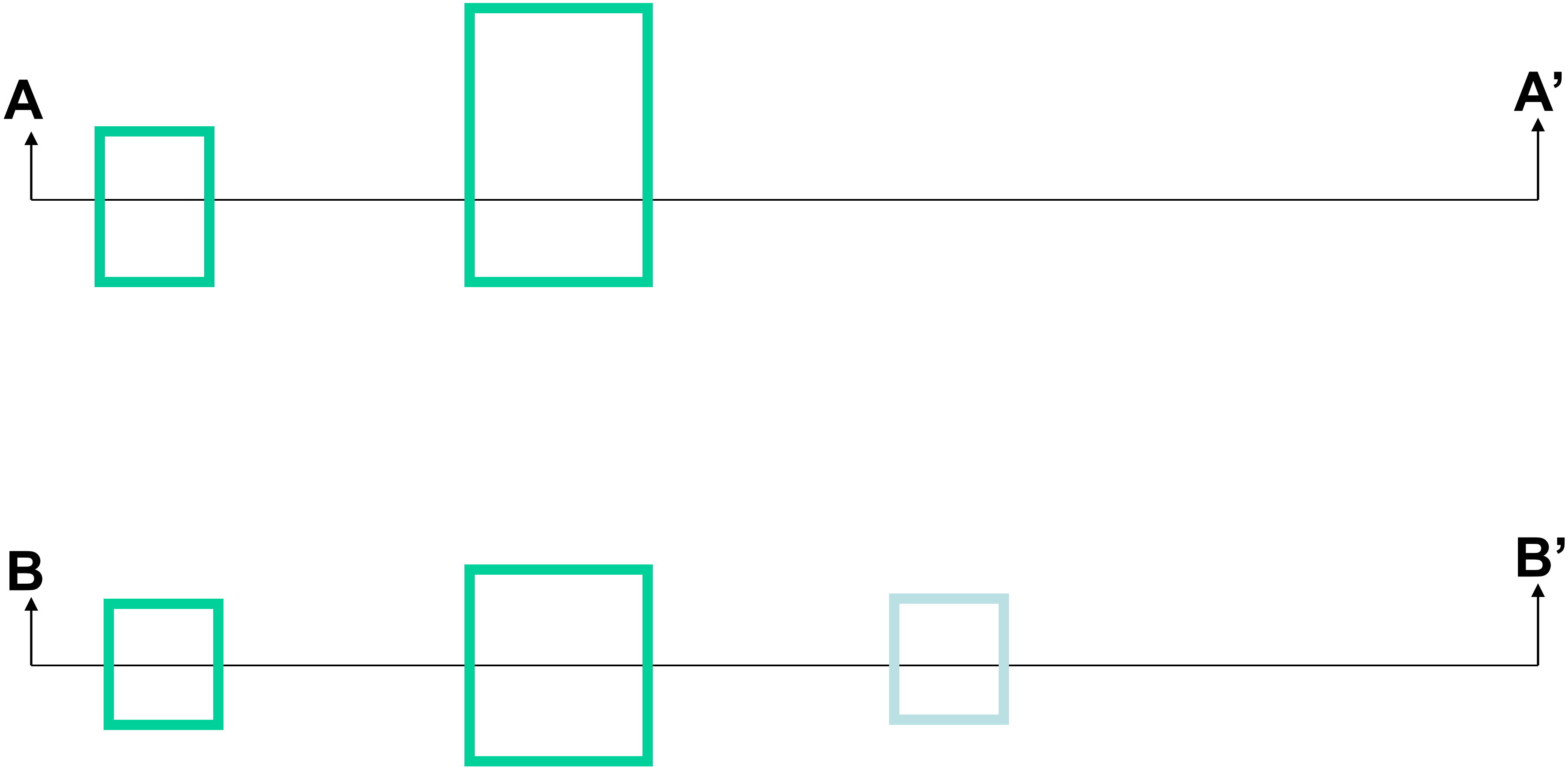
Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale



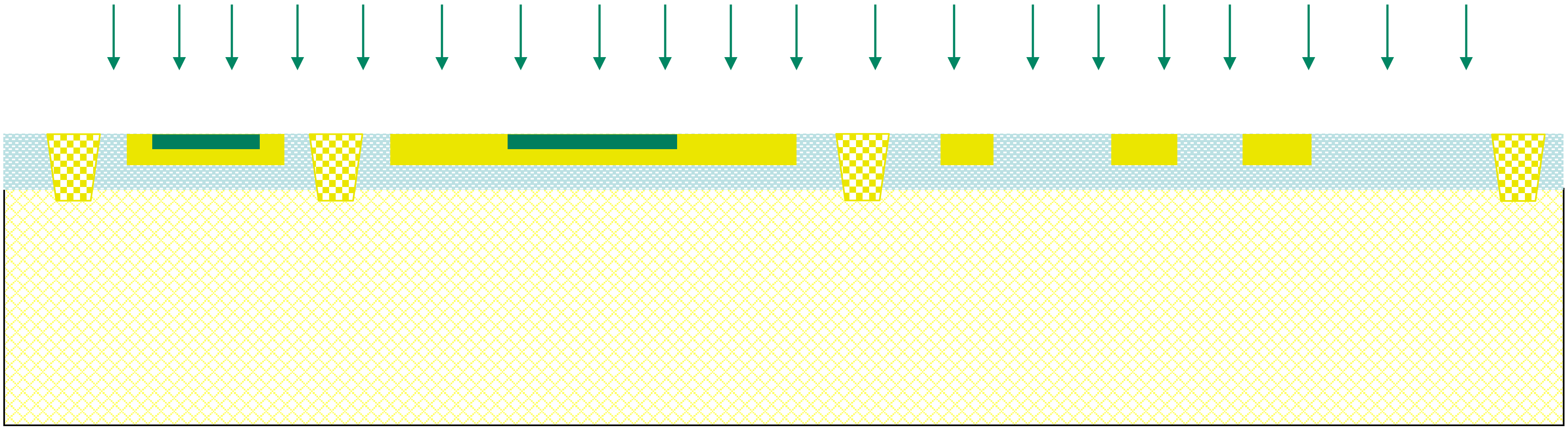
n^+ emitter diffusion

Mask 4: n^+ emitter diffusion

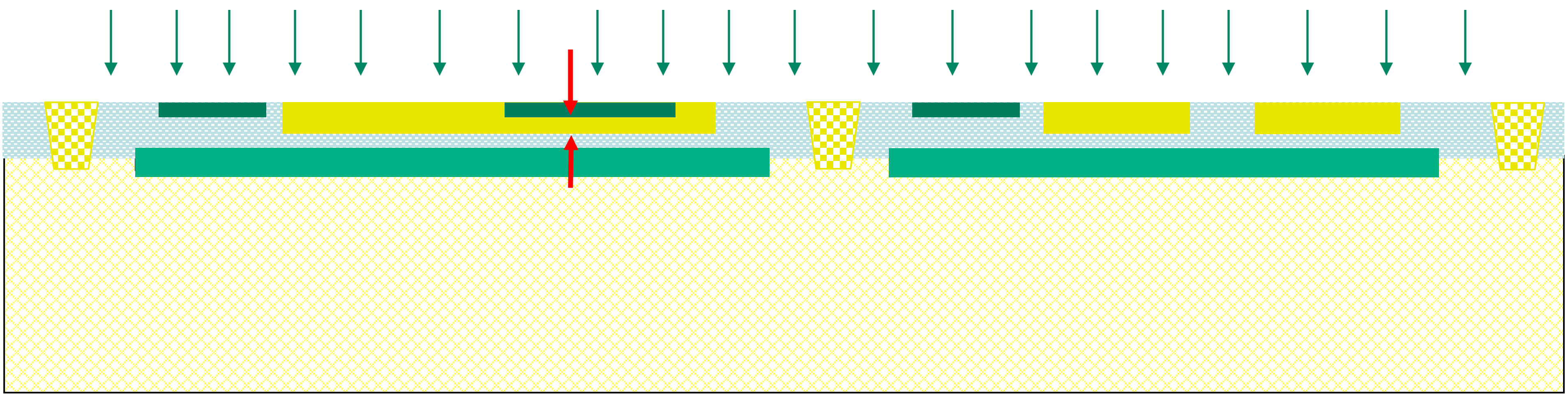


n⁺ emitter Diffusion

- Photoresist present but not shown
- Deposition and diffusion combined in slides



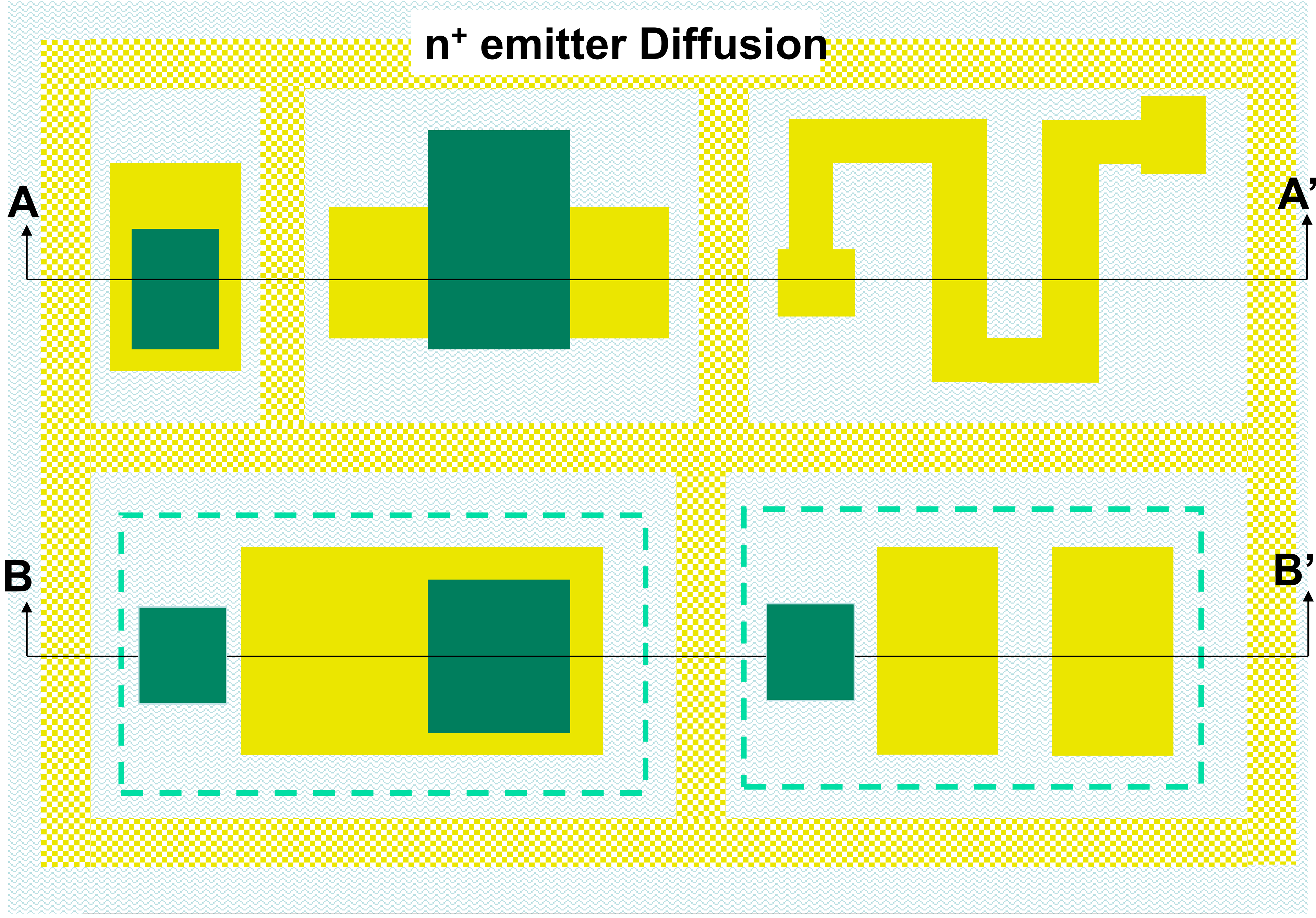
A-A' Section



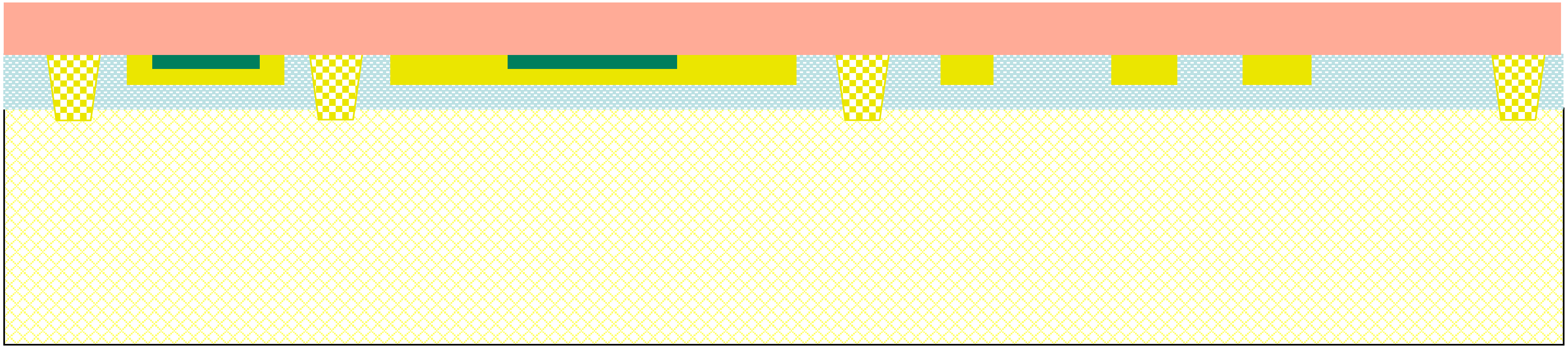
B-B' Section

Emitter diffusion typically leaves only thin base area underneath

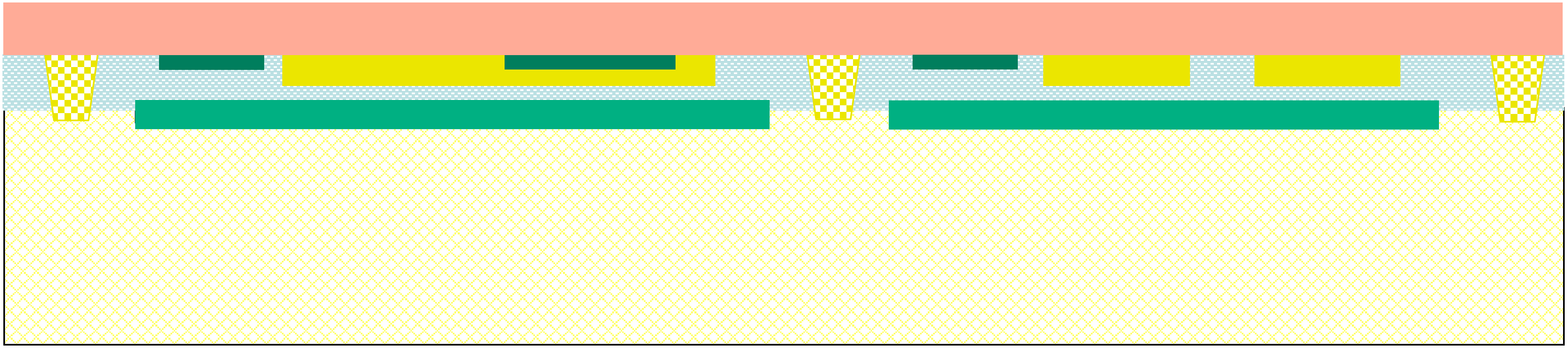
n+ emitter Diffusion



Oxidation

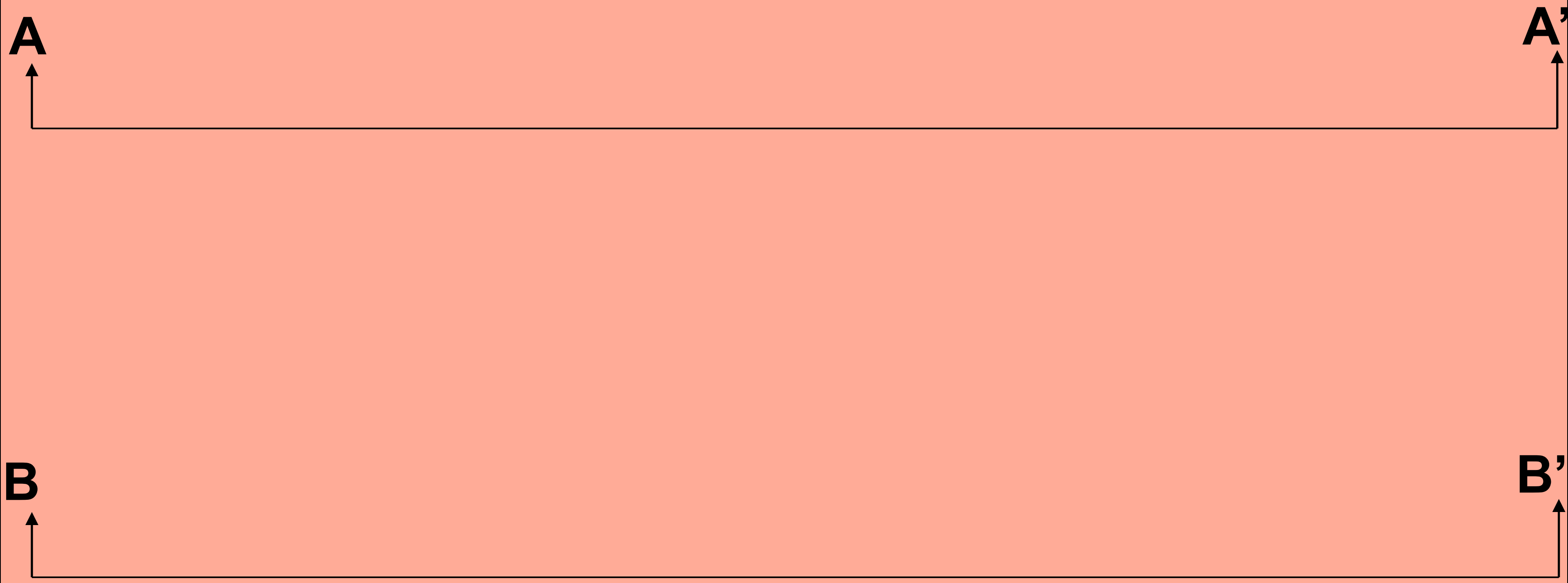


A-A’ Section



B-B’ Section

Oxidation

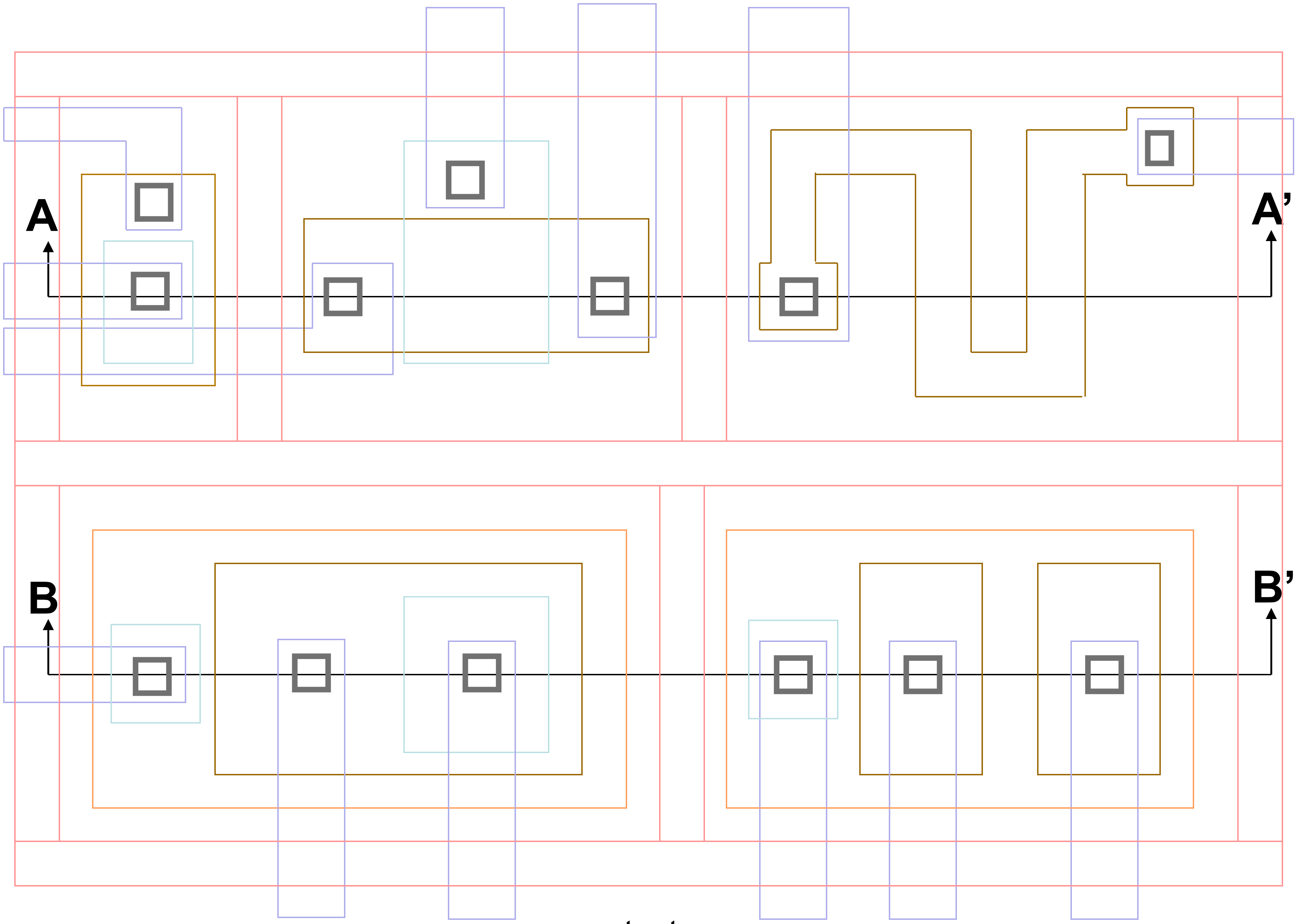


Mask Numbering and Mappings

Mask 1	n^+ buried collector
Mask 2	isolation diffusion (p^+)
Mask 3	p-base diffusion
Mask 4	n^+ emitter
Mask 5	contact
Mask 6	metal
Mask 7	passivation opening

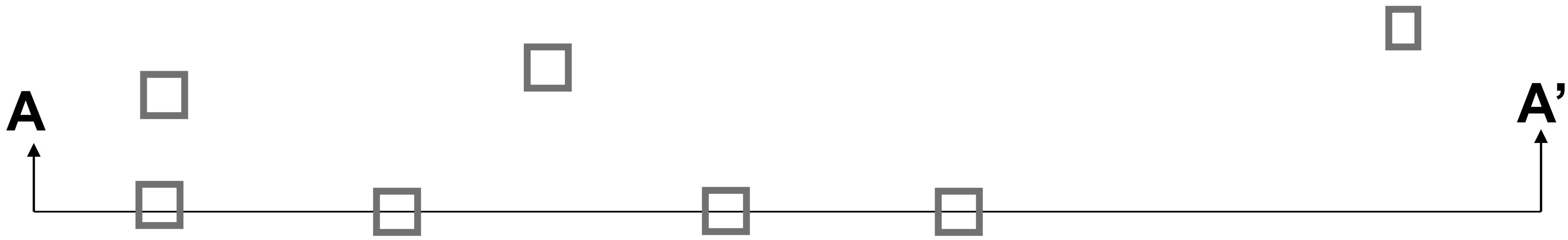
Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale



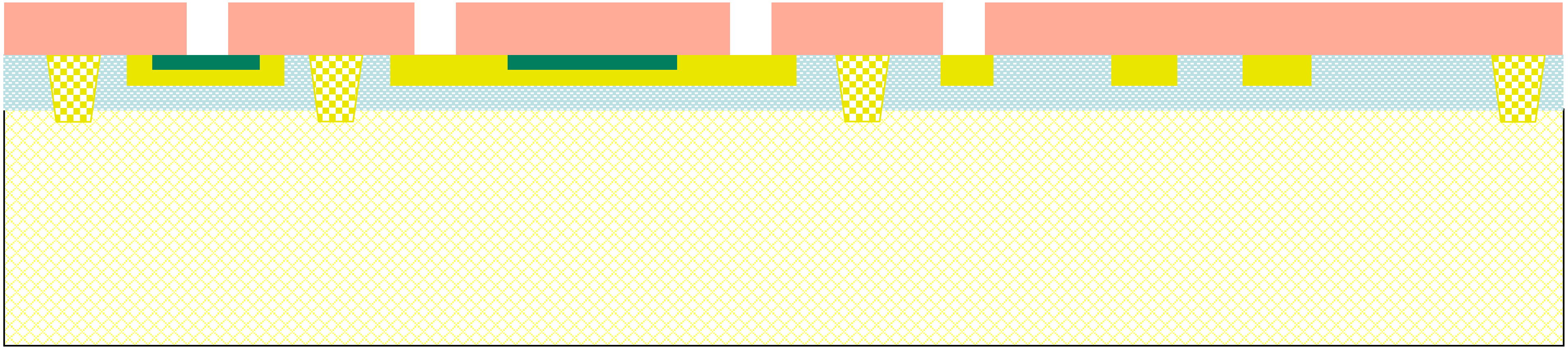
contacts

Mask 5: contacts

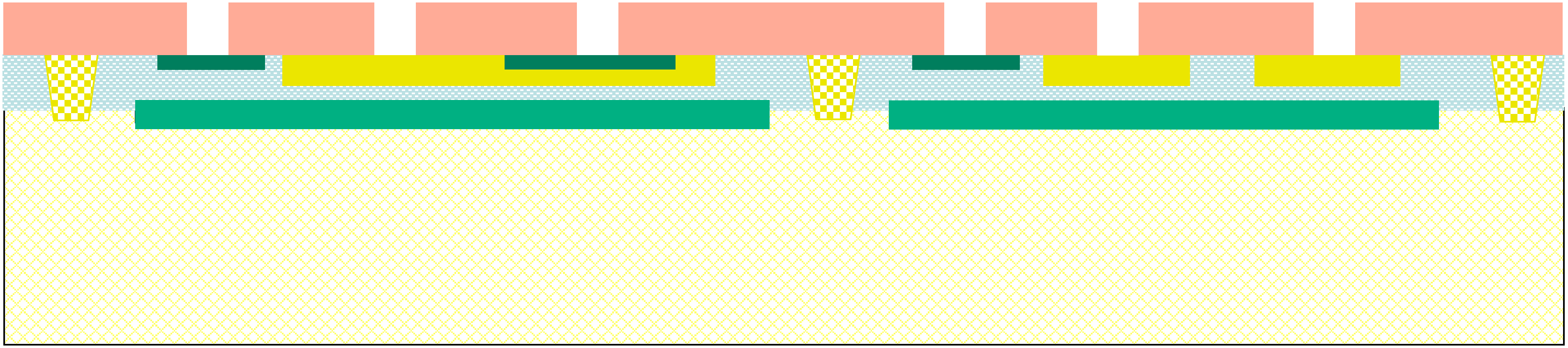


Contact Openings

- Photoresist present but not shown
- Deposition and diffusion combined in slides

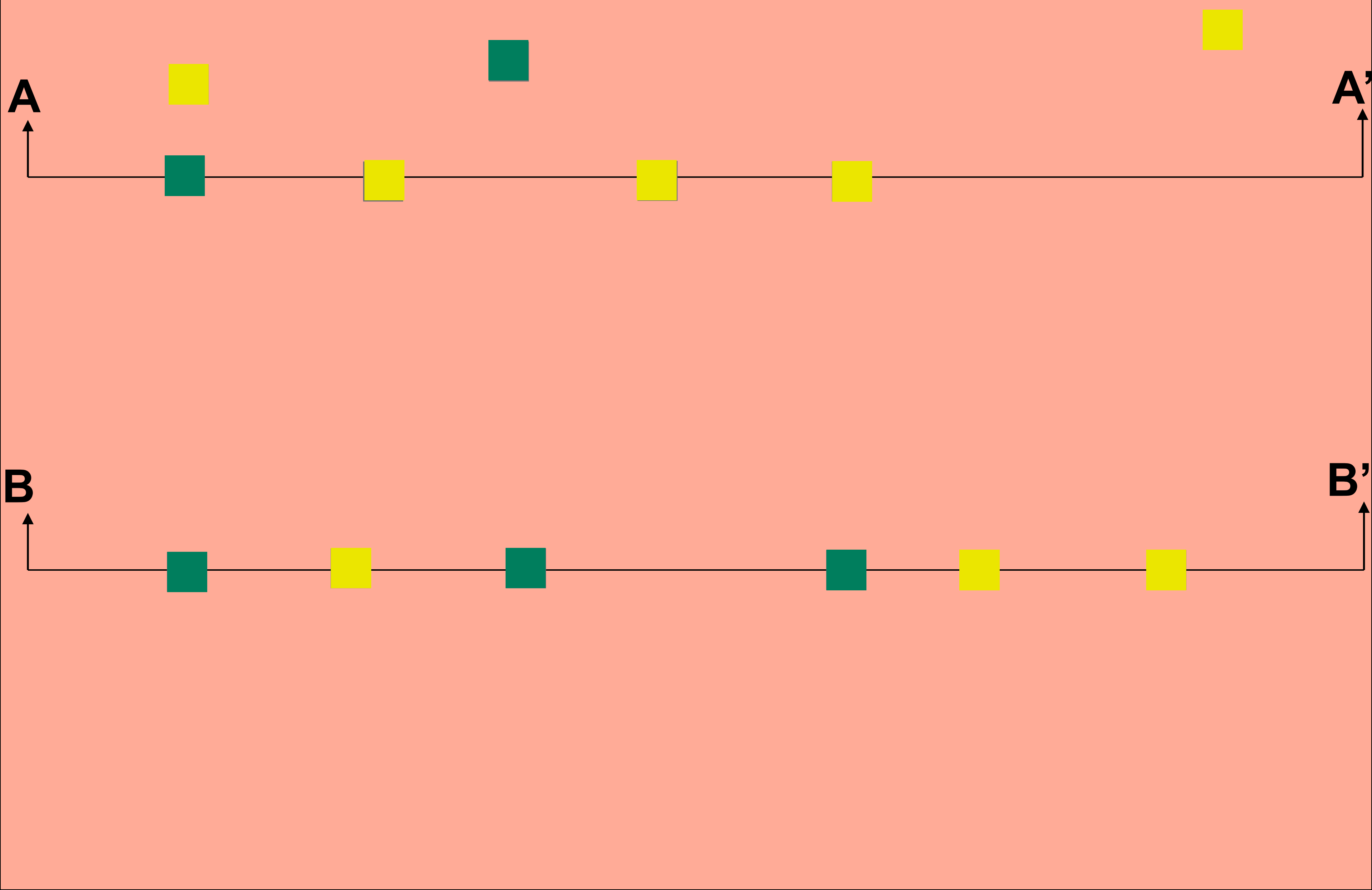


A-A’ Section



B-B’ Section

Contact Openings

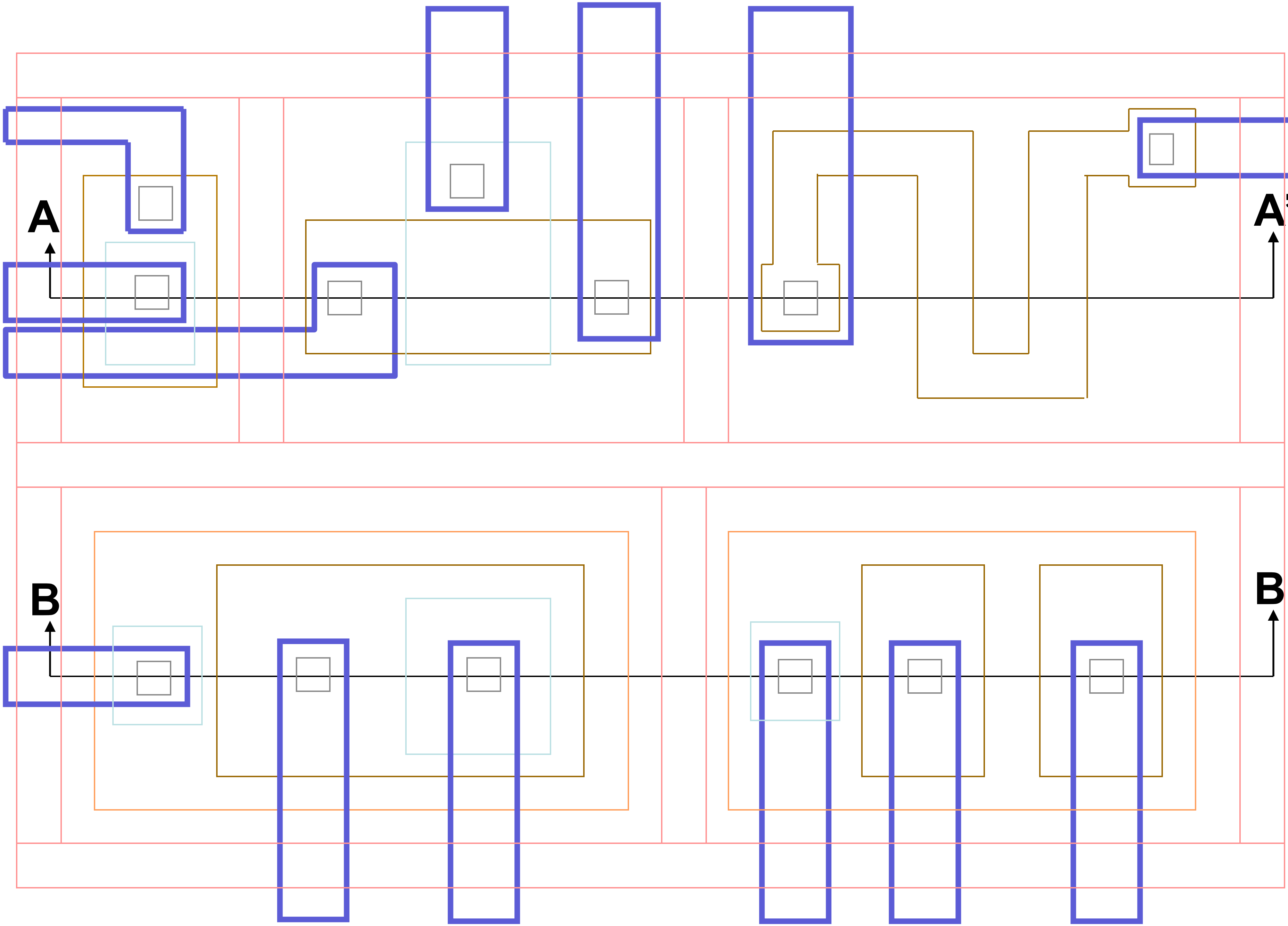


Mask Numbering and Mappings

Mask 1	n^+ buried collector
Mask 2	isolation diffusion (p^+)
Mask 3	p-base diffusion
Mask 4	n^+ emitter
Mask 5	contact
Mask 6	metal
Mask 7	passivation opening

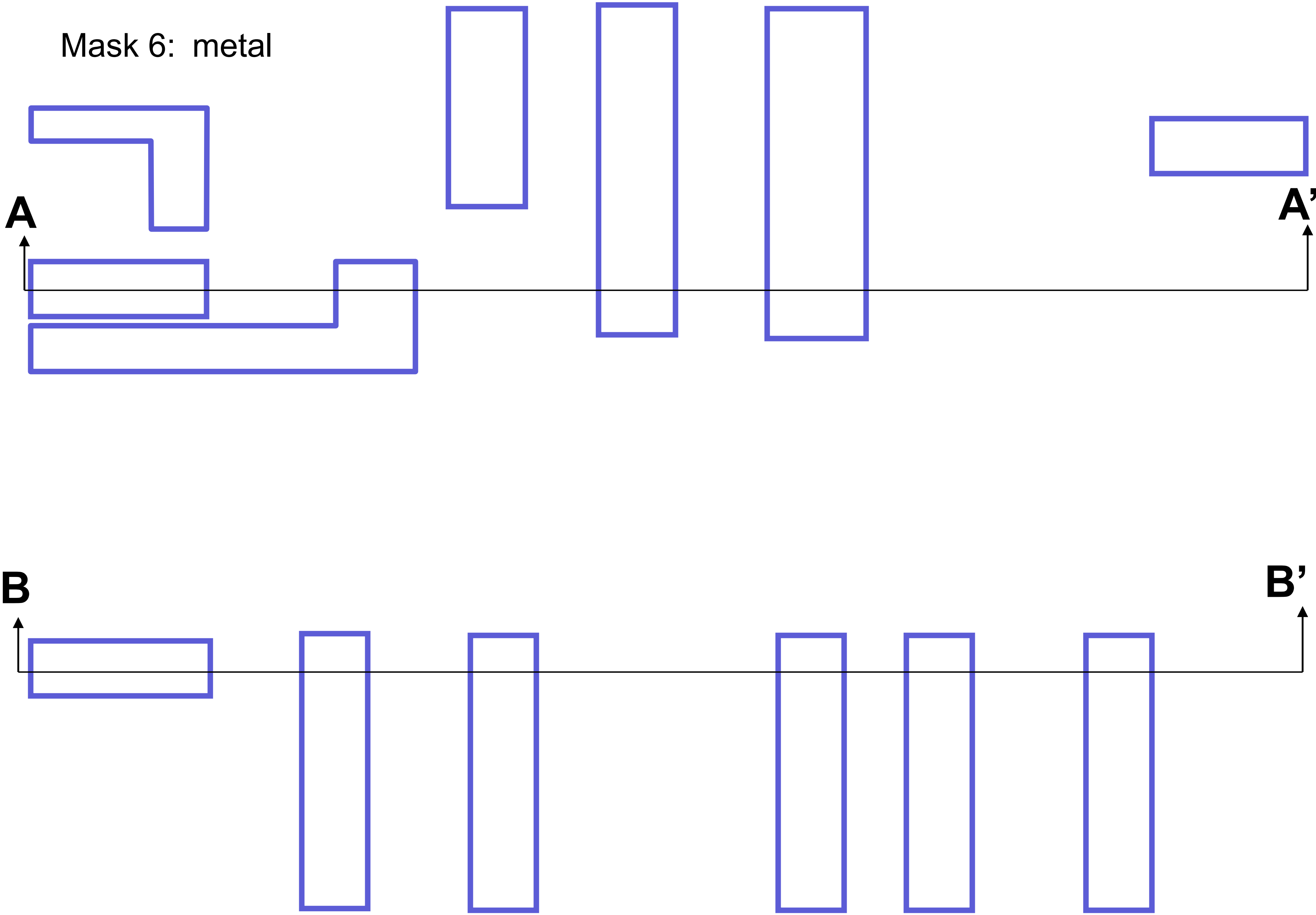
Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale



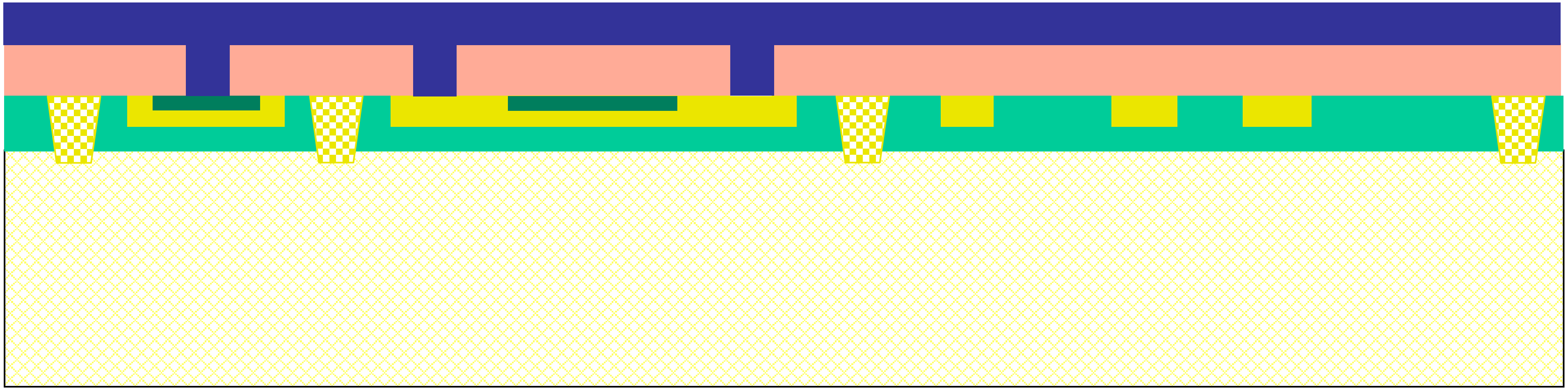
metal

Mask 6: metal

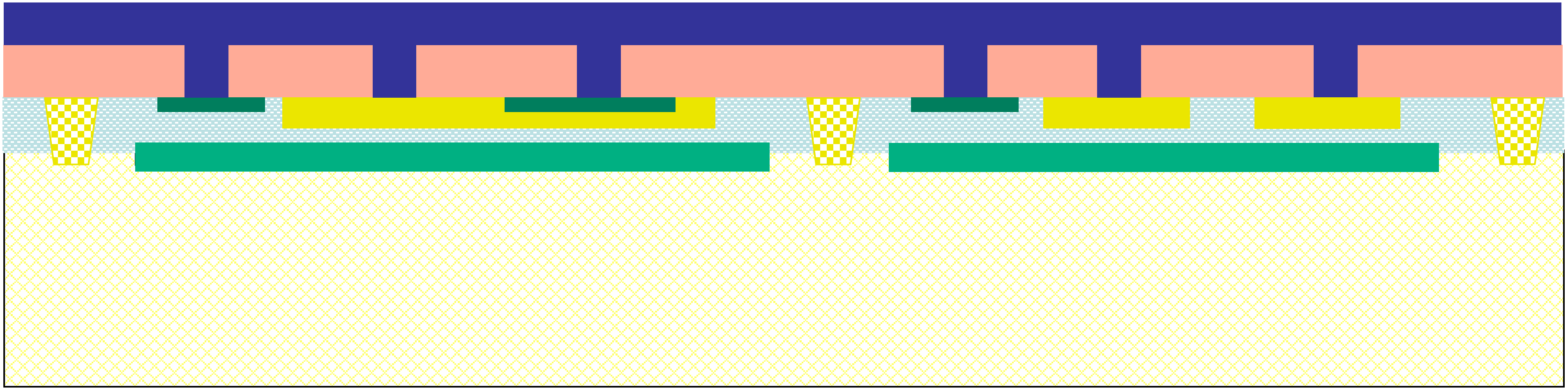


Metalization

- Photoresist present but not shown

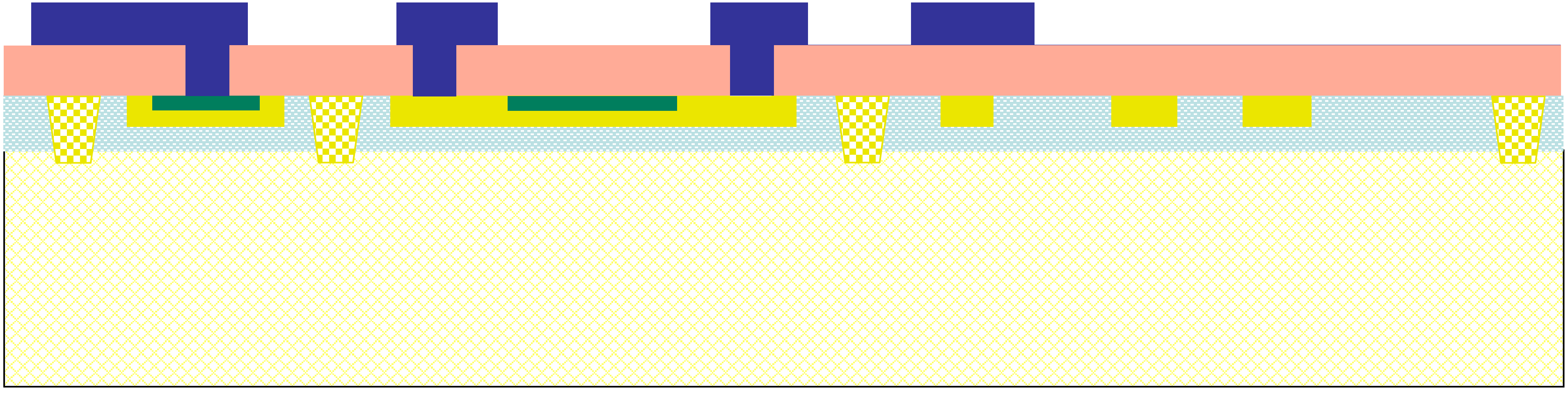


A-A' Section

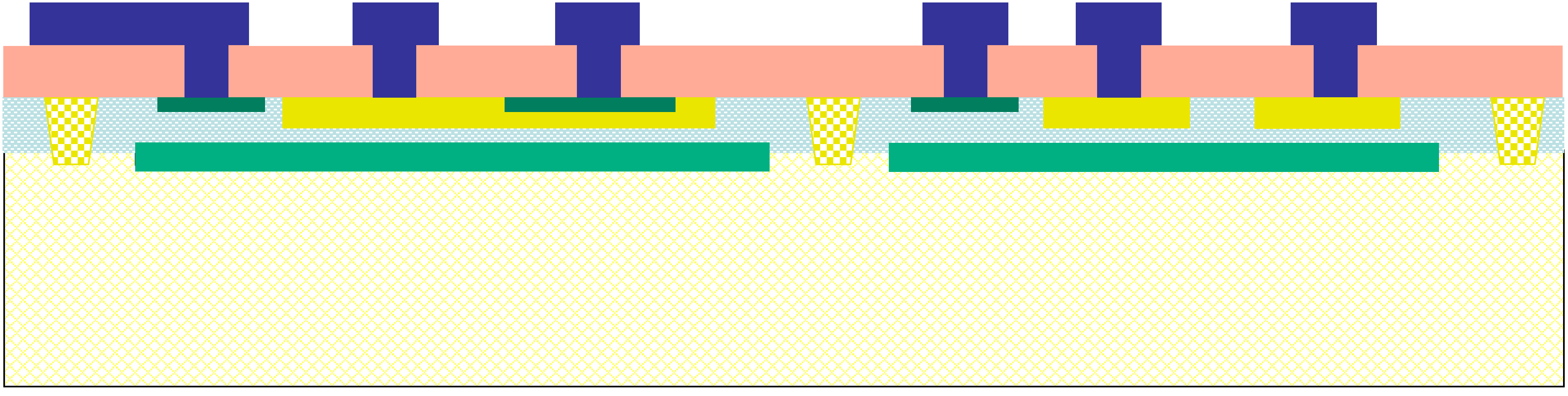


B-B' Section

Pattern Metal

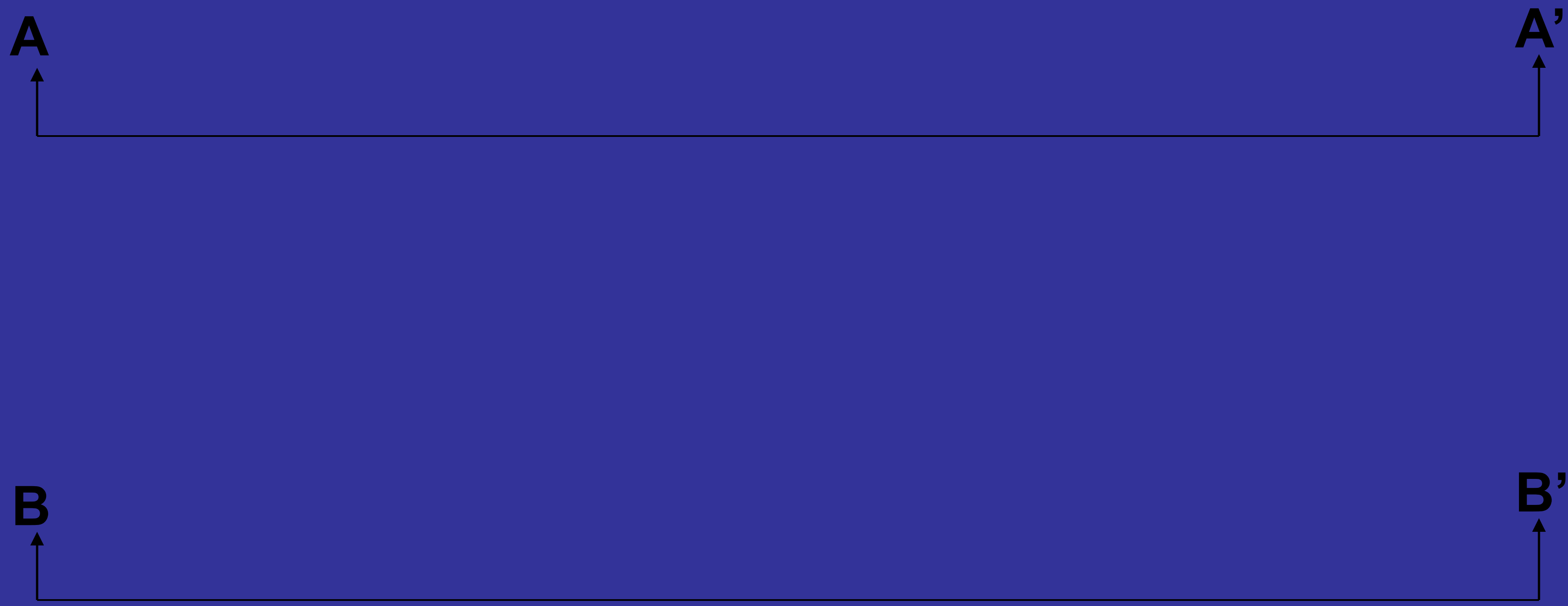


A-A' Section

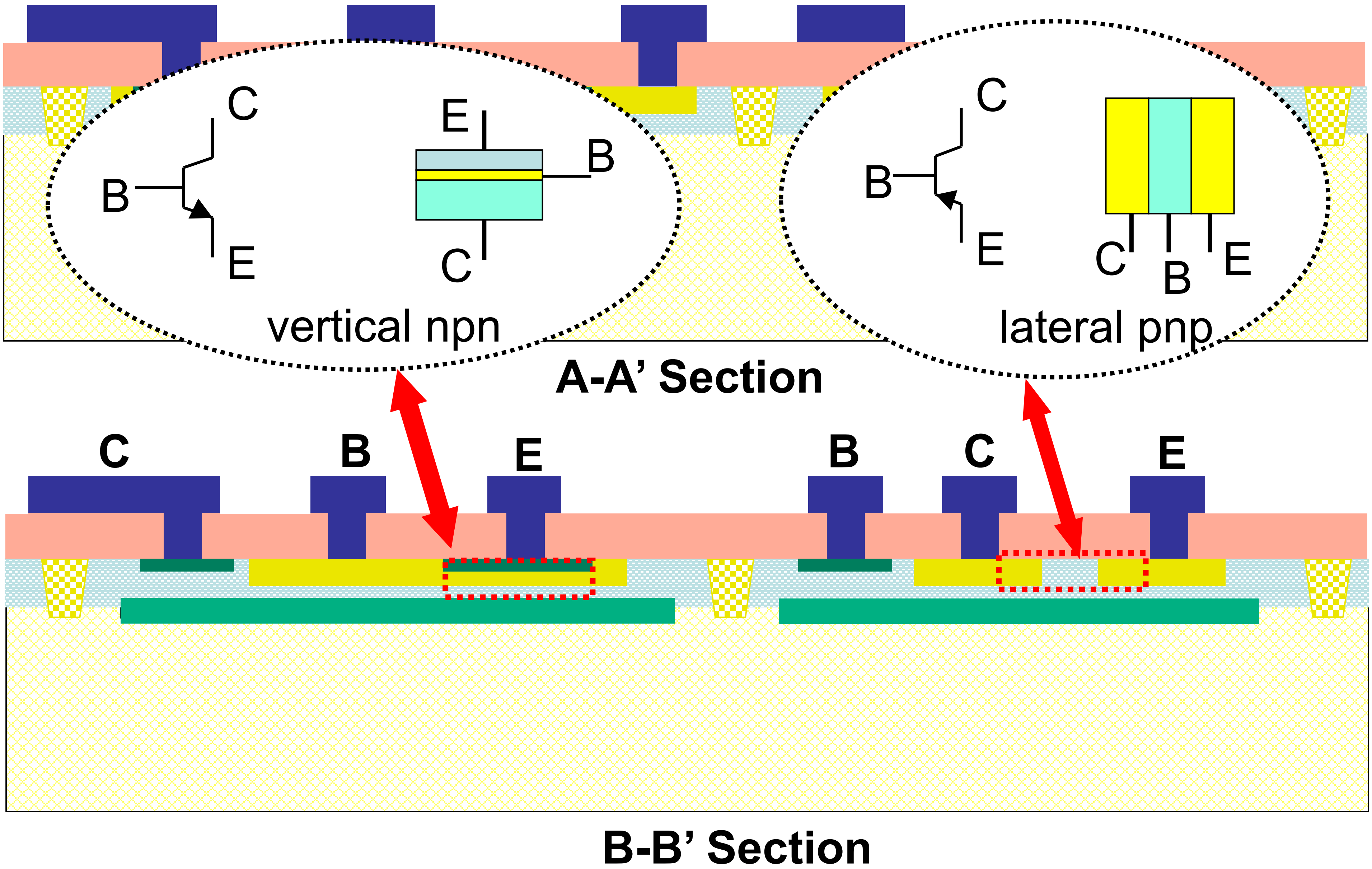


B-B' Section

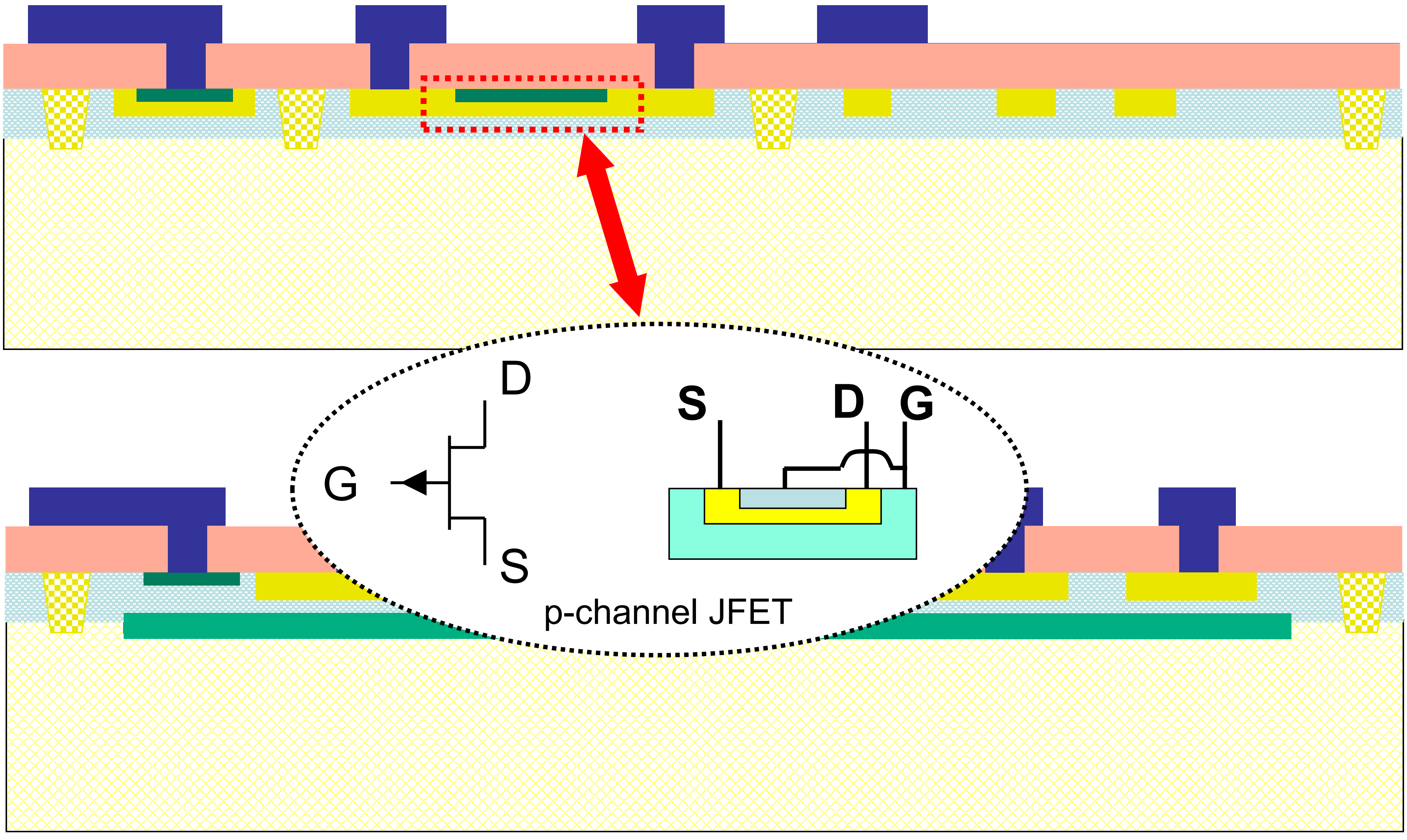
Metalization



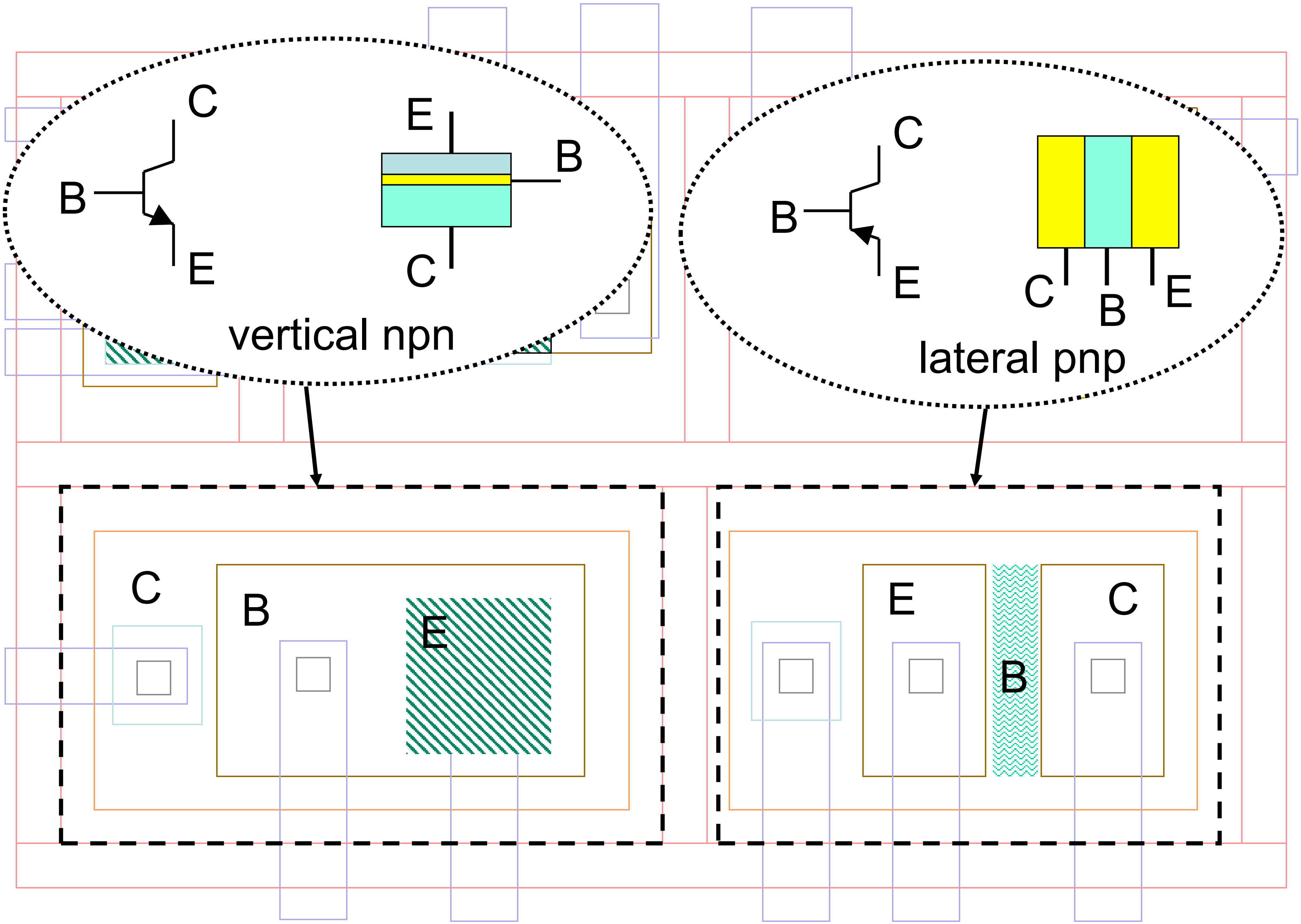
Pattern Metal

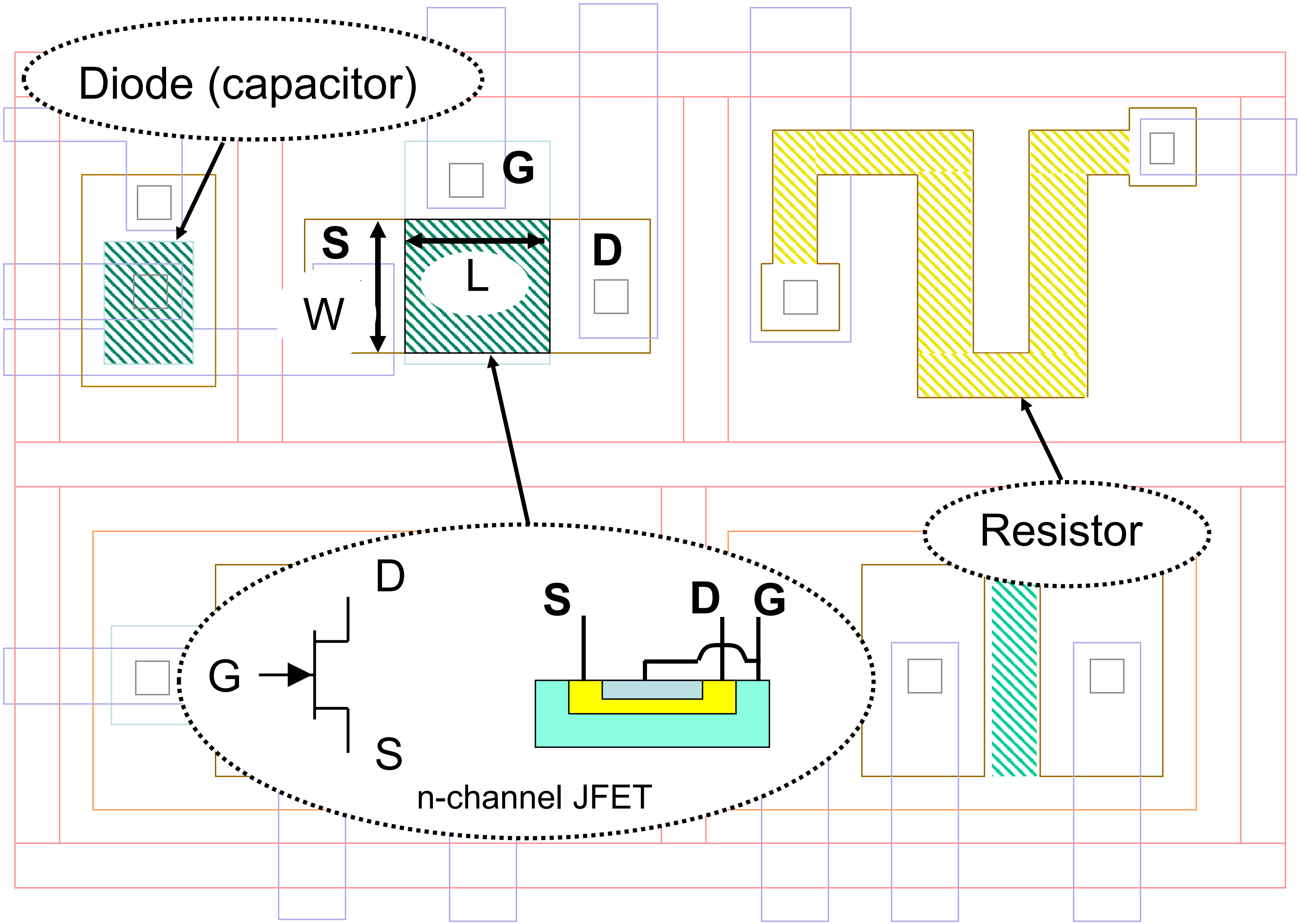


C
B
E
E
B
C
vertical npn
C
B
E
C
B
E
lateral pnp
A-A' Section
C
B
E
B
C
E
B-B' Section



B-B' Section


C
B
E
E
B
C
vertical npn
C
B
E
C
B
E
lateral pnp
C
B
E
E
C
B



Diode (capacitor)
G
S
D
L
W
Resistor
D
G
S
S
D
G
n-channel JFET

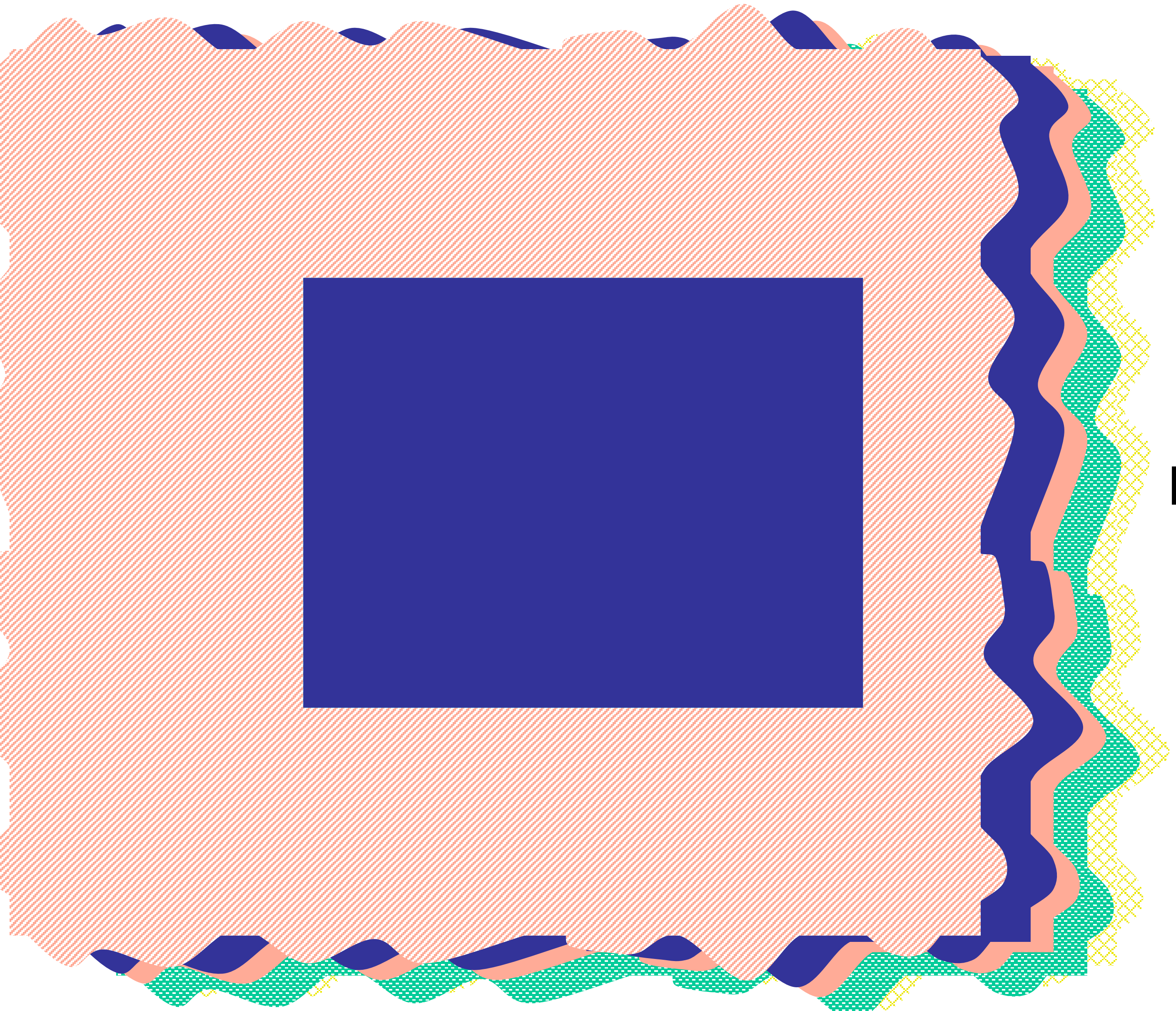
Mask Numbering and Mappings

Mask 1	(orange line)	n^+ buried collector
Mask 2	(red line)	isolation diffusion (p^+)
Mask 3	(brown line)	p-base diffusion
Mask 4	(green line)	n^+ emitter
Mask 5	(black line)	contact
Mask 6	(blue line)	metal
→ **Mask 7**	(cyan line)	passivation opening

Notes:

- passivation opening for contacts not shown
- isolation diffusion intentionally not shown to scale

Pad and Pad Opening



p-substrate

Epitaxial Layer

Oxidation

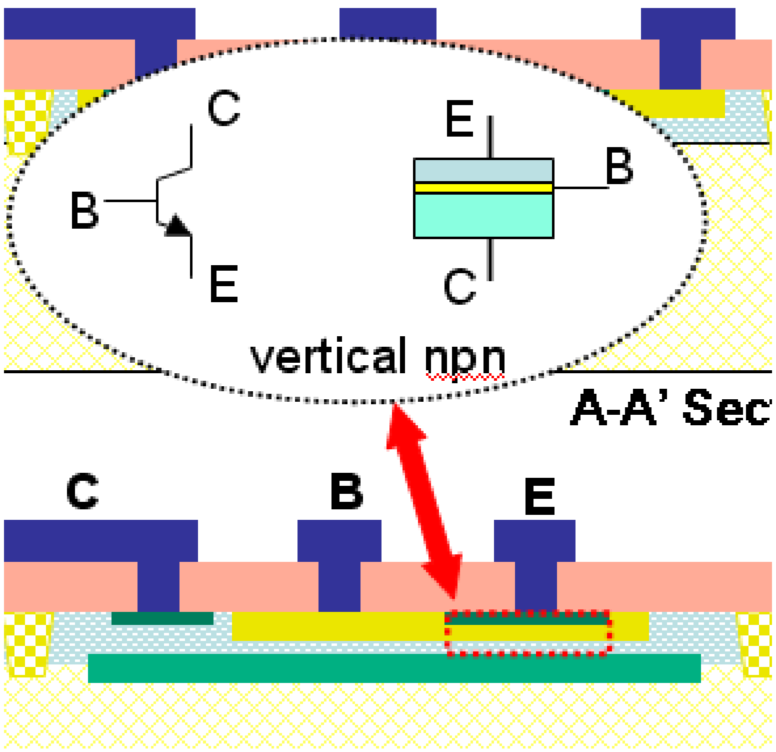
Metalization

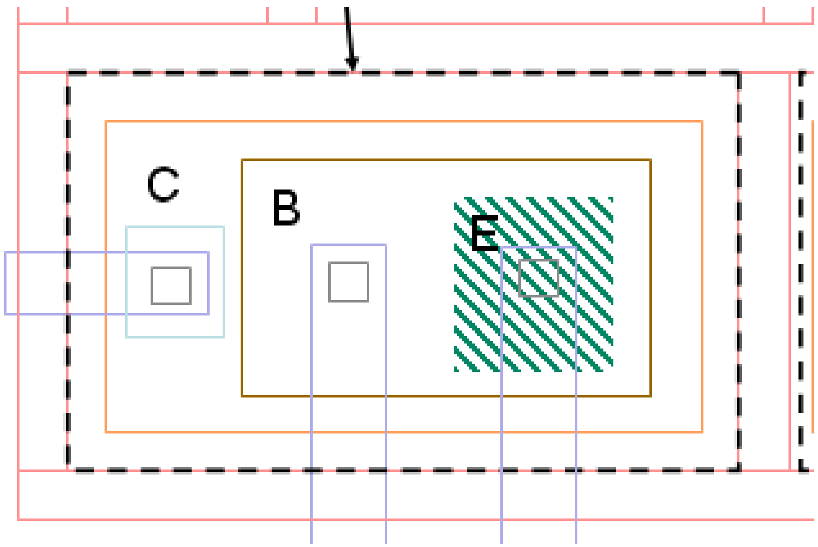
Protective Layer

Pad Opening Mask

Pad Opening

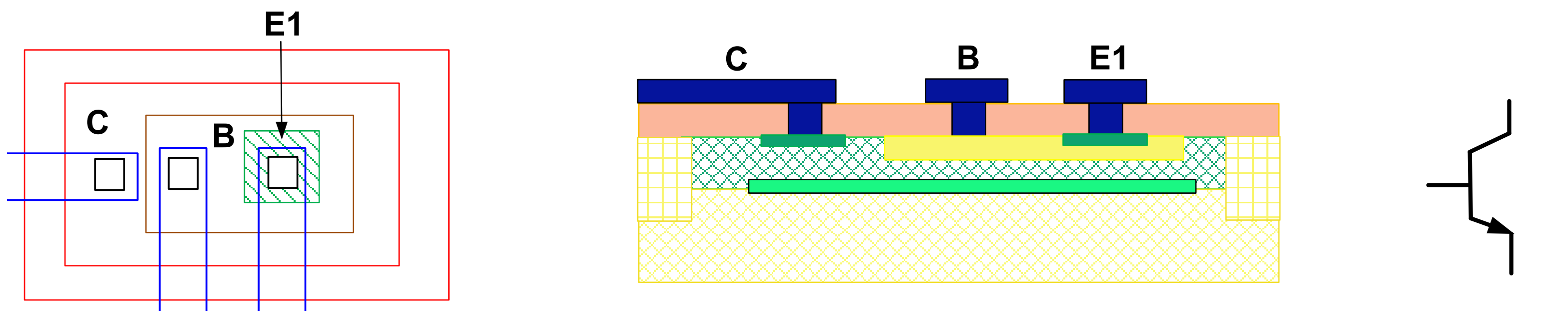
The vertical npn transistor

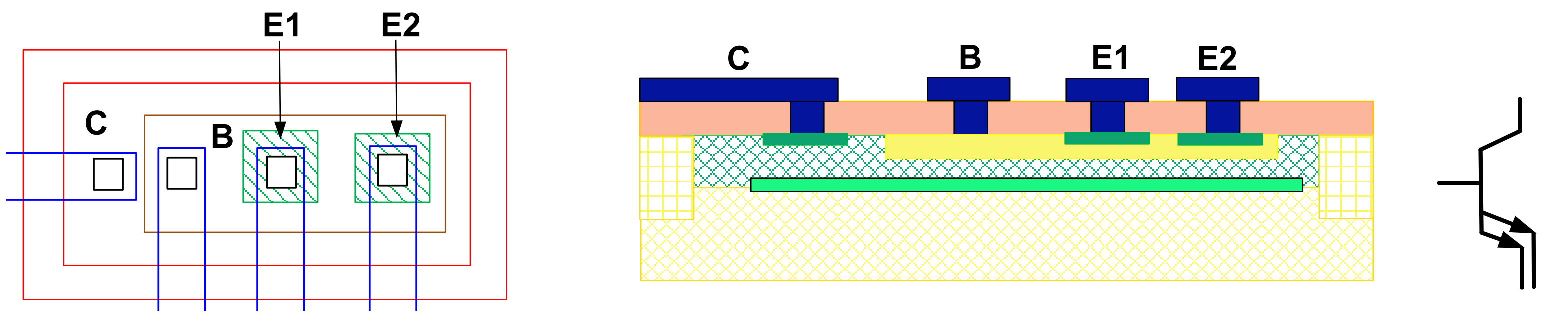




- Emitter area only geometric parameter that appears in basic device model !
- B and C areas large to get top contact to these regions
- Transistor much larger than emitter
- Multiple-emitter devices often used (TTL Logic) and don't significantly increase area
- Multiple B and C contacts often used (and multiple E contacts as well if A_E large)

The vertical npn transistor





Single-emitter and Double-Emitter Transistor

Base and Collector are shared

Quirks in modeling the BJT

[a] Parameters are defined in Chapters 3 and 4.

[b] Some of these Gummel-Poon parameters differ considerably from those given in Table 2C.4. They have been obtained from curve fitting and should give good results with computer simulations. The parameters of Table 2C.4 should be used for hand analysis.

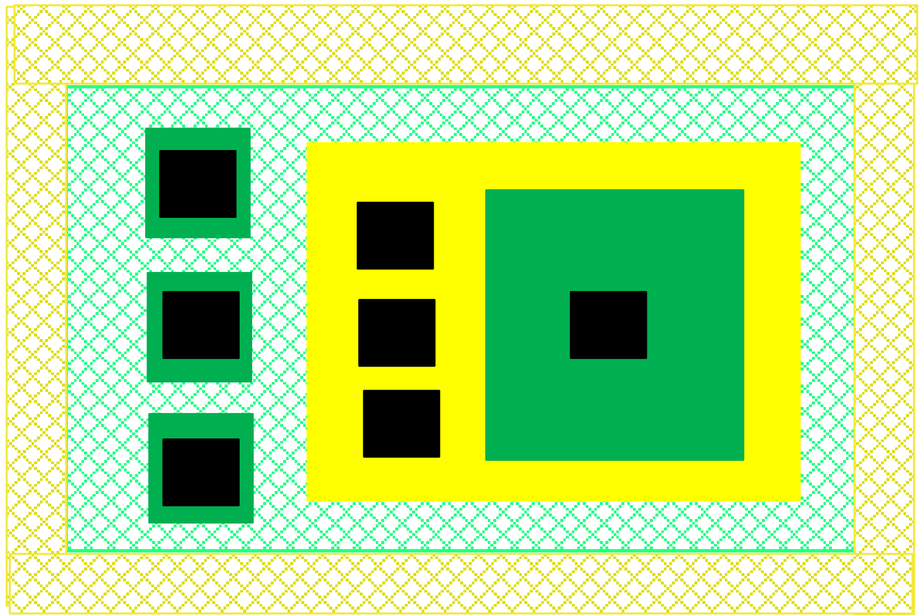
[c] Parameters that are strongly area-dependent are based upon an npn emitter area of 390 μ^2 and perimeter of 80 μ, a base area of 2200 μ^2 and perimeter of 200 μ, and a collector area of 10,500 μ^2 and perimeter of 425 μ. The lateral pnp has rectangular collectors and emitters spaced 10 μ apart with areas of 230 μ^2 and perimeters of 60 μ. The base area of the pnp is 7400 μ^2 and the base perimeter is 345 μ.

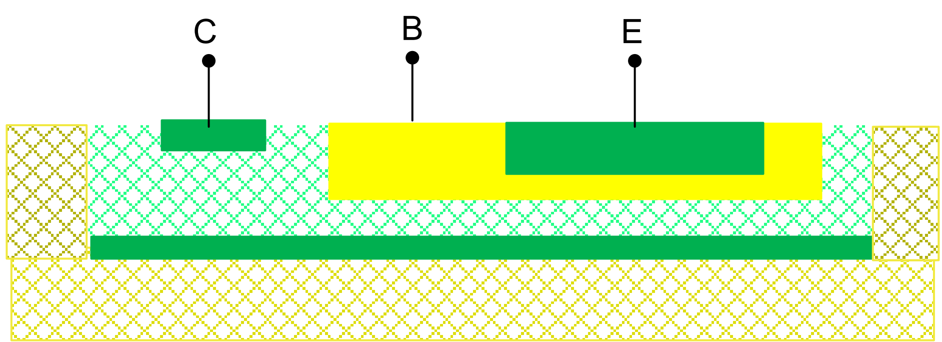
[d] CJS is set to zero for the lateral transistor because it is essentially nonexistent. The parasitic capacitance from base to substrate, which totals 1.0 pF for this device, must be added externally to the BJT.

- In contrast to the MOSFET where process parameters are independent of geometry, the bipolar transistor model is for a specific transistor !
- Area emitter factor is used to model other devices
- Often multiple specific device models are given and these devices are used directly
- Often designer can not arbitrarily set A_E but rather must use parallel combinations of specific devices and layouts

A challenge in modeling the BJT

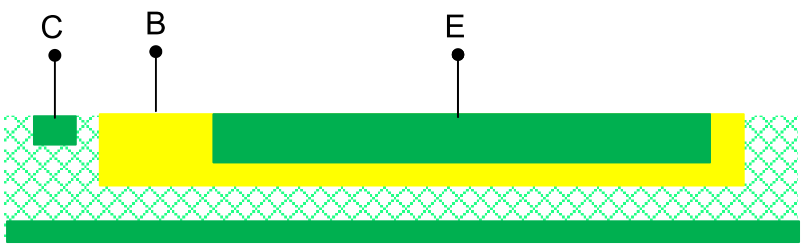
Top View of Vertical npn

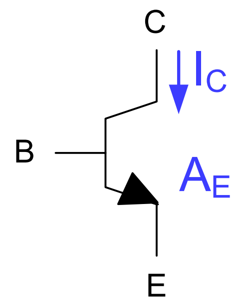




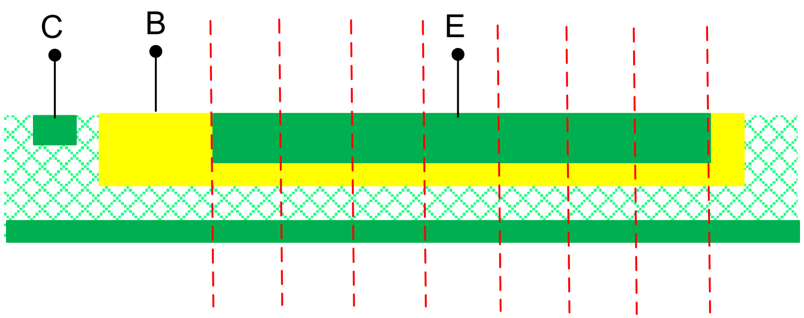
Cross-Sectional View

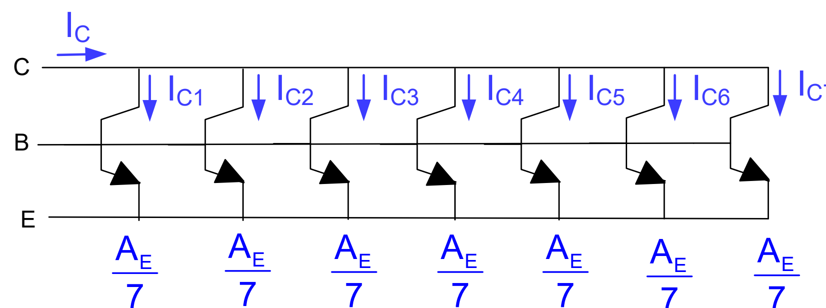
A challenge in modeling the BJT





$$I_C = A_E J_S e^{\frac{V_{BE}}{V_t}}$$





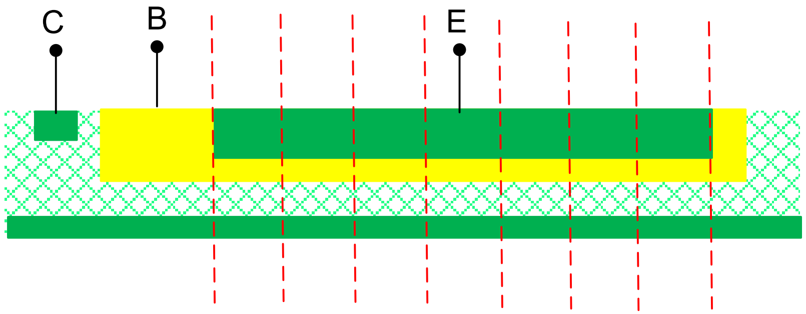
$I_{C1} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C3} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C5} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C7} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$

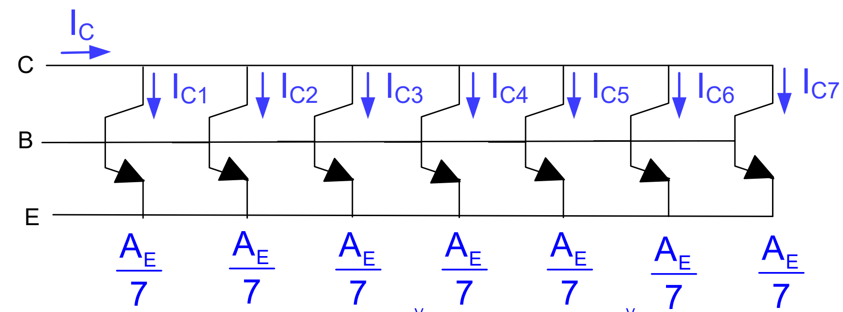
$I_{C2} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C4} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C6} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$

$$I_C = \sum_{i=1}^{7} \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}} = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

This looks consistent but …

A challenge in modeling the BJT





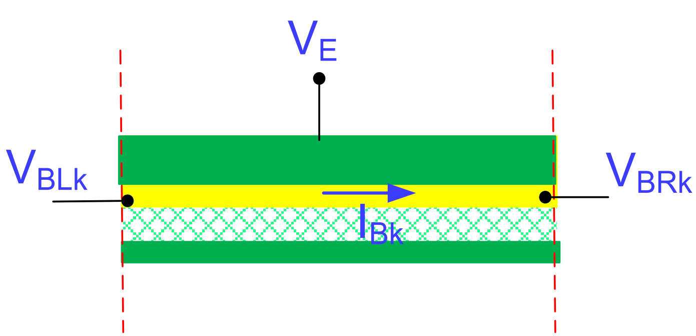
$I_{C1} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C3} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C5} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C7} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$

$I_{C2} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C4} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$ $I_{C6} = \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}}$

$$I_C = \sum_{i=1}^{7} \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}} = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

This looks consistent but …

consider an individual slice

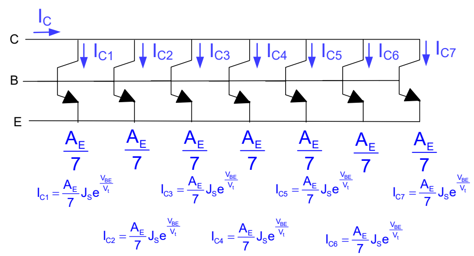


Lateral flow of base current causes a drop in base voltage across the base region

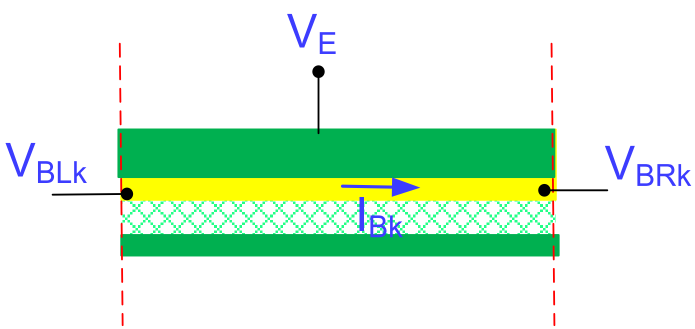
$$V_{BRk} \neq V_{BLk} \qquad I_{Ck} = \frac{A_E}{7} J_S e^{\frac{V_{BEk}}{V_t}}$$

What is V_{BEk}?

A challenge in modeling the BJT



This looks consistent but …



$$I_C = \sum_{i=1}^{7} \frac{A_E}{7} J_S e^{\frac{V_{BE}}{V_t}} = A_E J_S e^{\frac{V_{BE}}{V_t}}$$

- Lateral flow of base current causes a drop in base voltage across the base region
- And that drop differs from one slice to the next
- So V_{BE} is not fixed across the slices
- Since current is exponentially related to V_{BE}, affects can be significant
- Termed **base spreading resistance** problem
- Causes "**Current Crowding**"
- Base resistance and base spreading resistance both exist and represent different phenomenon
- Strongly dependent upon layout and contact placement
- No good models to include this effect
- Major reason designer does not have control of transistor layout detail in some bipolar processes
- Similar issue does not exist in MOSFET because the corresponding gate voltage does not change with position since I_G=0

A challenge in modeling the BJT

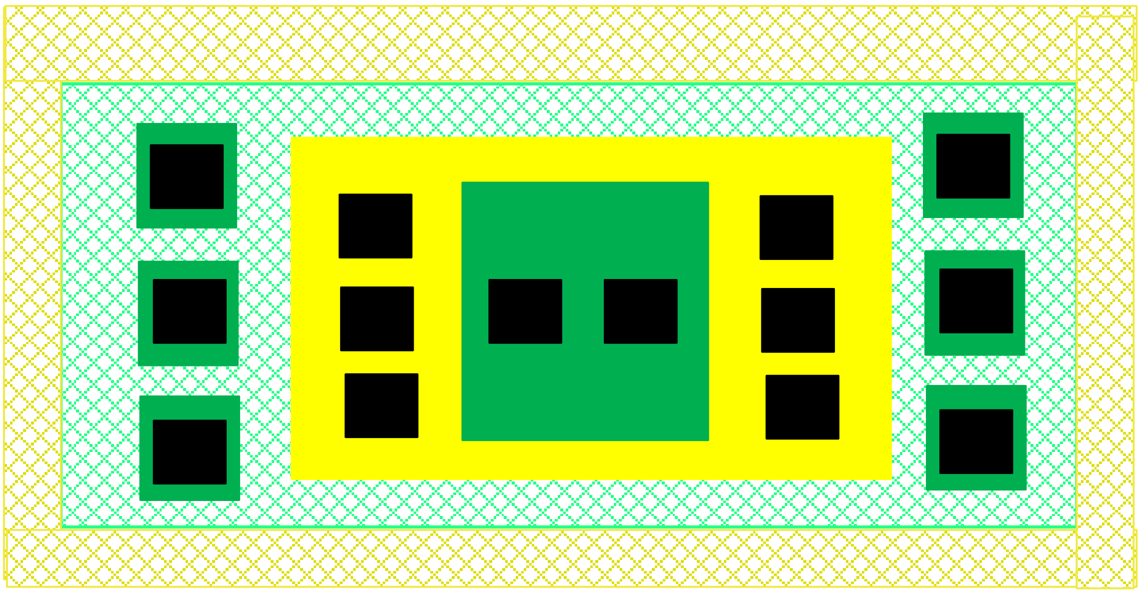
Top View of Vertical npn

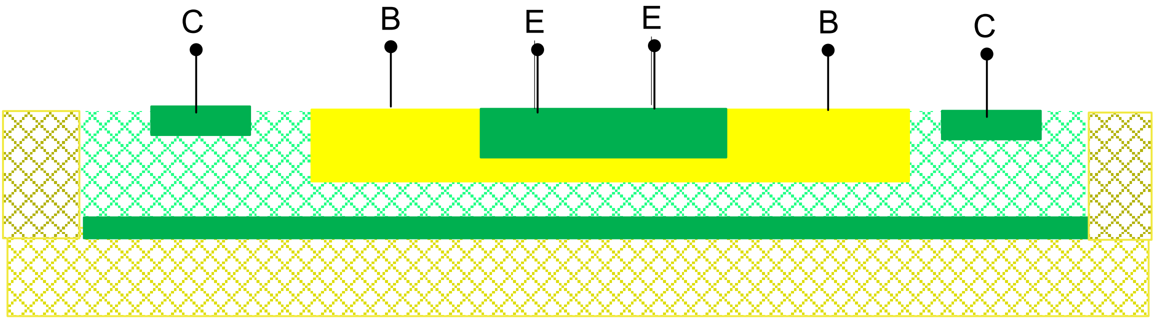
Cross-Sectional View

A challenge in modeling the BJT

What can be done about this problem ?

Top View of Vertical npn



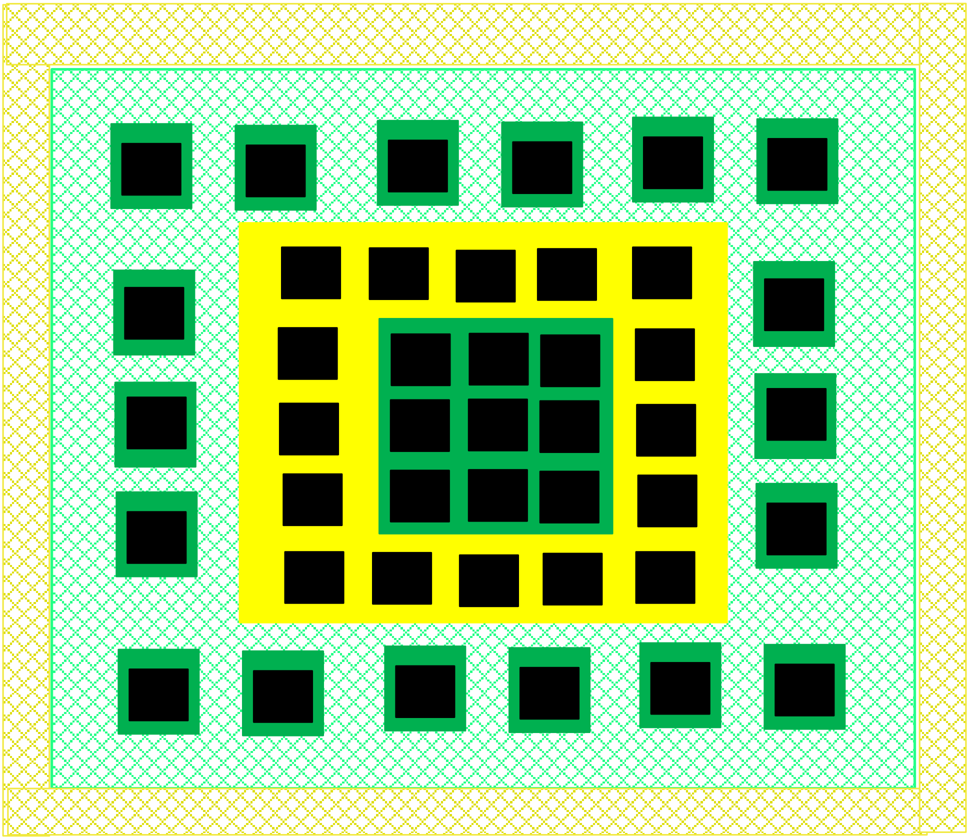


Cross-Sectional View

A challenge in modeling the BJT

What can be done about this problem ?

Top View of Vertical npn



- Often double rows of contacts used
- Area overhead can be significant
- Effects can be reduced but current flow paths are irregular
- Remember **emitter area** is key design variable

MOS and Bipolar Area Comparisions

How does the area required to realize a MOSFET compare to that required to realize a BJT?

Will consider a minimum-sized device in both processes

Stay Safe and Stay Healthy !

End of Lecture 21